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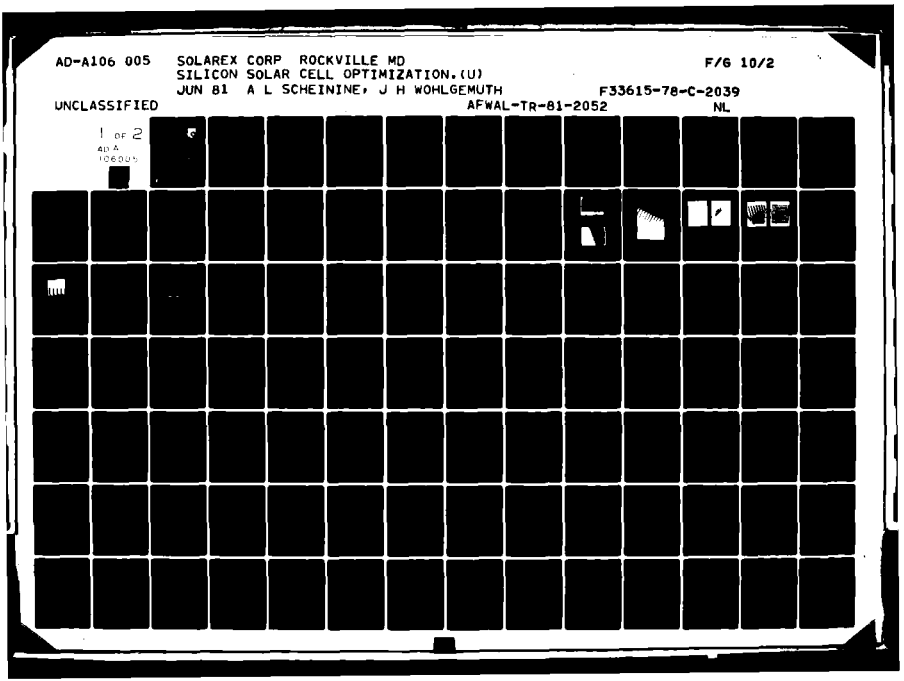

AFWAL-TR-81-2052

SILICON SOLAR CELL OPTIMIZATION

SOLAREX CORPORATION
1335 PICCARD DRIVE
ROCKVILLE, MARYLAND 20850

June 1981

Final Report for Period August 1978 - February 1981

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This technical report has been reviewed and is approved for publication.

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This research program has resulted in improvements in vertical junction solar cell techniques leading to higher efficiencies and improved handleability. Vertical junction solar cells have now been fabricated with AM0 conversion efficiency greater than 15% (25°C). A variety of cells have been fabricated including different groove depths, substrate thicknesses and bulk resistivities. Cell performance has been measured both before and

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after irradiation. Theoretical analysis has been performed to generate computer models of I-V curves for various cell geometries.

FOREWORD

This Technical Report covers all work performed under Contract No. F33615-78-C-2039, entitled "Silicon Solar Cell Optimization". The effort was sponsored by the Aero Propulsion Laboratory, AF Wright Aeronautical Laboratories Air Force Systems Command, Wright-Patterson Air Force Base, Ohio under Project 3145. Mr. J. Beam (AFWAL/POOC) and Lt. K. Masloski were the Air Force Project Engineers. Dr. John Wohlgemuth of Solarex Corporation was Program Manager, while Mr. Alan Scheinine served as principal investigator.

The work reported herein was performed during the period 15 August 1978 to 15 February 1981.

The authors wish to thank Dr. Patrick Rahilly and Dr. George Storti for helpful suggestions and Mr. Donald Warfield, Ms. Eileen Sparks and Mr. R. Edwards for cell fabrication.

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SECTION 1

INTRODUCTION

The goal of this program is to improve the beginning-of-life (BOL) AM0 efficiency of silicon solar cells without sacrificing the radiation resistance so that a significant improvement in the end-of-life (EOL) efficiency can be obtained. Solarex has elected to use the vertical junction (VJ) cell structure for this program since it results in cells that are more radiation-resistant than other silicon structures. Therefore, improvements in BOL efficiency will result in higher EOL efficiency.

The vertical junction solar cell is made from a silicon slice with grooves etched into one surface. Grooves on the order of 5 microns wide spaced 15 to 20 microns apart are etched in the surface in a regular pattern. Figure 1 shows such a VJ structure. The diode junction follows the surface of the silicon up and down the walls. Since the walls are very narrow, carriers generated in the walls by incident light are always close to the collecting junction. Even if the carrier diffusion length is reduced, carriers created in the walls are able to traverse the short distance to the junction and be collected. Therefore, the vertical junction cell has the inherent capability of providing superior radiation resistance.

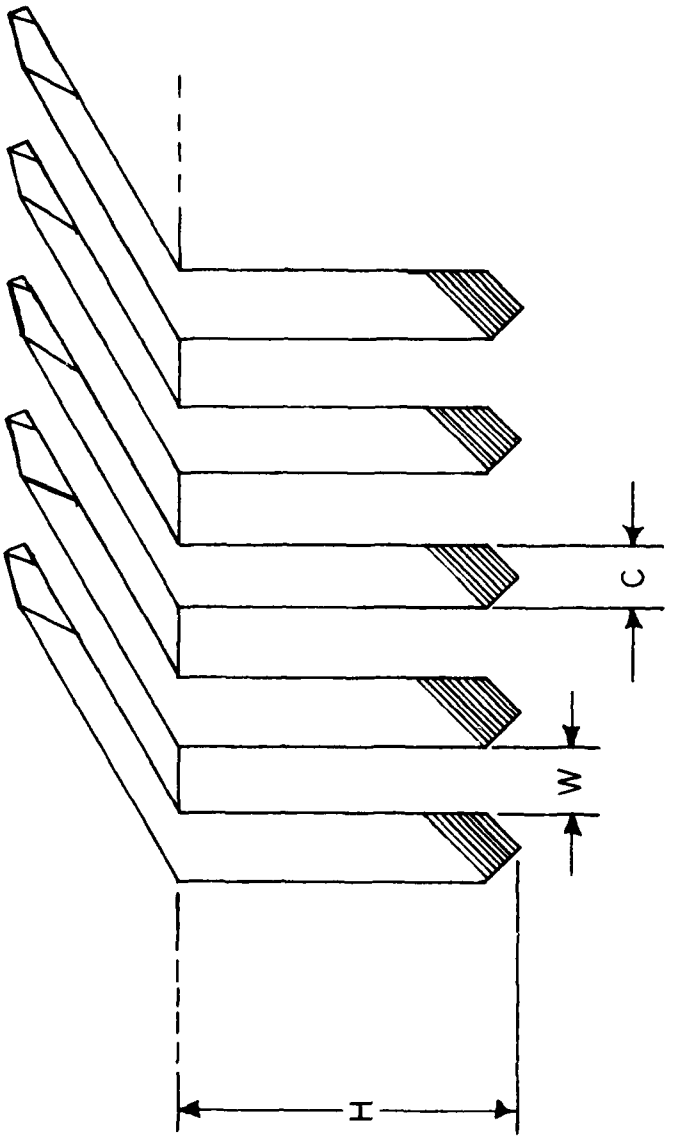


Figure 1. Structure of Vertical Junction Solar Cell

Vertical junction cells have been fabricated with AM0 efficiencies greater than 15%. This improvement has been obtained by the use of new geometries, improved back surface field formation, the use of a back surface reflector and the use of double-layer AR coatings. The use of new cell geometries has enabled the fabrication of cell assemblies that can withstand thermal cycling and can be handled and connected by conventional techniques. These characteristics will allow VJ cells to be used in space arrays.

Thinning techniques have been employed to produce VJ cells with as little as 50 microns of silicon below the bottom of the grooves. This not only results in lightweight cells but improves the radiation resistance beyond that of a full-thickness VJ cell. This work has also shown that a highly polished silicon surface is not required for VJ fabrication: a standard chem-mechanical polish is adequate for the required photolithography.

The fabrication processes for VJ cells have been well documented in the literature (References 1 through 4). A brief description of the process techniques, with emphasis on new developments or modifications, is presented in Section 2. These new developments have simplified the process, providing for faster throughput and higher yields.

The experimental results are described in Section 3. Characteristics of a variety of VJ structures are presented along with details of their performance after particulate irradiation. In addition, information on cell assemblies, such as optical performance, are presented.

During this program, theoretical analysis has resulted in the development of computer-generated I-V curves for specific cell geometries and performance parameters. Comparison of theoretical and experimental performance has led to iterations in the modeling and identification of areas where the model does not correctly predict device performance. Section 4 describes the theory behind the model, the mathematics behind the computer programs and the predictions of the model for various cell structures.

The final section summarizes the development of this program and suggests the efforts required to reach the program goal of 18% BOL AM0 efficiency.

SECTION 2

EXPERIMENTAL PROCEDURES

The techniques for formation of the vertical junction structure have been developed in earlier efforts (Ref. 1-4). Refinements in processing have contributed to improved cell performance and function. Experimentation and methods of fabrication are described in the following sections: (1) Substrate Thinning, (2) VJ Structure Formation, (3) Cell Fabrication and (4) Coversliding. The process sequence is shown in Figure 2.

(1) Substrate Thinning

Silicon wafers are easily thinned and simultaneously polished by etching in a mixture of 3:5:6 parts by volume of 48% HF, 70% HNO_3, and 98% CH_3COOH (Chemical Polish #26). When properly activated, this etchant removes silicon at a rate of approximately one micron per second without regard to crystal orientation. The desired substrate thickness is then easily attained by etching for a specified time period. By this method, silicon wafers have been obtained at 3,5, and 7 mils from the standard 12 mil stock. The surface that results from this etch is mirror-polished and sufficiently defect-free that no further surface treatment is needed prior to VJ structure formation.

GROOVE WAFER

CUT WAFER

CLEAN WAFER

GROW OXIDE

PHOTOLITHOGRAPHY:

APPLY RESIST

EXPOSE RESIST

DEVELOP RESIST

PAINT BACK

OXIDE ETCH, HF, buffered

GROOVE ETCH, KOH

WALL POLISHING ETCH, CP

15 - 120 sec.

DIFFUSION, JUNCTION

DIFFUSION:

PHOSPHINE GASEOUS SOURCE

840°C to 870°C

REMOVE PHOSPHORUS GLASS

MEASURE SHEET RESISTANCE

Figure 2. Process Sequence

BACK SURFACE FIELD

SCREEN PRINT AL PASTE

ALLOY:

IN AIR

800°C TO 900°C

BACK CLEAN-UP, HCL & HF

FRONT METALLIZATION

INSERT WAFERS INTO SHADOW MASKS

OR

PHOTOLITH DEFINE FRONT CONTACTS

VACUUM EVAPORATION OF METAL, TiPd

(LIFT-OFF PHOTORESIST)

BACK SURFACE REFLECTOR

ULTRASONIC CLEAN

VACUUM EVAPORATE ALUMINUM

METALLIZATION CONTINUED

VACUUM EVAPORATE BACK METAL, TiPd

CHECK ADHESION

ELECTROPLATE SILVER

SILVER ETCH $NH_4OH:H_2O_2$ 8:1

Figure 2. Process Sequence (continued)

AR COATING

CUT WAFERS

CLEAN WAFERS

VACUUM EVAPORATE TiO_2 OR Ta_2O_5

SINTER:

450°C IN AIR, 20 - 30 SEC

VACUUM EVAPORATE MGF_2 OR Al_2O_3

SINTER:

450°C IN AIR, 20 - 60 SEC

TEST

Figure 2. Process Sequence (continued)

(2) Vertical Junction Structure Formation

The fabrication of vertical junction cells requires the formation of deep grooves into the surface of the silicon substrate. The process which makes this technically possible is the orientation-dependent etch. Kendall (Ref. 5) found that the etch rate of silicon in KOH varies by as much as 400 times, depending upon crystal orientation. During the orientation etch, the <111> plane etches more slowly than the other planes. Therefore, the silicon wafer must have <111> planes normal to the surface in order to generate the desired grooves, and the surface orientation of silicon wafers is necessarily the <110> plane.

Since <110> ingots are hard to grow dislocation-free, the best source of <110> wafers is from <111> ingots which are X-ray aligned and cut perpendicular to the <111> axis, leaving <110> wafers. To facilitate alignment of the etching mask to the <111> planes, a flat is cut on the <111> plane.

(a) Wafer Cleaning

The surfaces of silicon wafers must be smooth and free from contamination prior to any processing. The wafers are therefore:

- cleaned in a solution of 2:1 by volume H_2SO_4:H_2O_2
- etched in 1:1 HCl:H_2O
- etched in dilute HF

This treatment removes all organic, metallic, and oxide contaminants from the surface.

(b) Oxide mask formation

Etching grooves into the silicon requires an effective alkaline-resistant mask which will withstand the etching solution long enough that grooves of the required depth can be etched. The formation of the mask must not degrade the silicon in any way. The best method to accomplish this task involves growing a phosphosilicate glass on the surface of the wafer by means of a short phosphorus diffusion followed by the growth of oxide in steam, all at a temperature of 850°C (Ref. 2).

Experimentally, the steam oxide period can be adjusted to make the oxide thick enough to withstand the etchant as long as needed to produce the desired groove depth.

(c) Groove pattern generation and orientation

Standard photolithographic techniques are used to generate the groove pattern on the surface of each wafer. Hexamethyldisilazane is used to improve the adhesion of the

photoresist to the oxide-coated wafer. The photolithography pattern is mechanically aligned to the <111> plane so the etch will produce deep, narrow grooves. Each wafer is exposed and developed using standard techniques. The resultant groove pattern is visible as windows of exposed oxide on the resist-coated wafer surface.

(d) Oxide etch

The photoresist remaining on the surface acts as a mask for the oxide etch. A solution of 6:1 parts by volume of NH_4F:HF is used to remove the exposed oxide from the silicon with minimal undercutting of the resist. After the oxide is completely removed from the groove pattern, the resist is removed in acetone. The resultant groove pattern is now visible as windows of clean silicon on the oxide-coated wafer surface.

(e) Groove etch

The orientation-dependent etchant found to yield the best results is 45% aqueous KOH at 70-75°C. Under these conditions, this etchant removes silicon from the groove pattern at a rate of approximately one micron/minute. The desired groove depth can be achieved by etching the oxide-masked wafers for a specified time period. Wafers have been fabricated with groove depths of 0.5, 1.0, 2.0, 3.0 and 4.0 mils, as needed. The resultant walls are extremely straight

and parallel with square tops (Figure 3). After the groove etch, the remaining oxide is removed by etching in a solution of 6:1 parts by volume of NH_4F:HF.

(f) Chemical polish/wall polish

During the oxide growth, phosphorus was diffused into the silicon wafers. Some of this phosphorus remains in the top of the walls. A chemical polish etch containing 1:3:8 parts by volume of 48% HF:70% HNO_3:98% CH_3COOH removes the top layer of silicon and simultaneously polishes the groove walls. A long etch in this solution (approximately 60 sec) has previously been used to round the wall tops to improve optical coupling. The resultant wall geometry is more fragile than desired and permits more incident light to impinge on the cell substrate rather than the walls. Therefore, a fifteen-second etch has been used for most cells, with improved optical coupling provided by a double layer AR coating (see Figure 4a and b).

3. Cell Fabrication

The grooved wafers are fabricated into solar cells by processes similar to those employed in the fabrication of planar wafers. The presence of multiple crystal planes as well as the need to diffuse down narrow grooves are unique features of the vertical junction cell but present few processing problems.

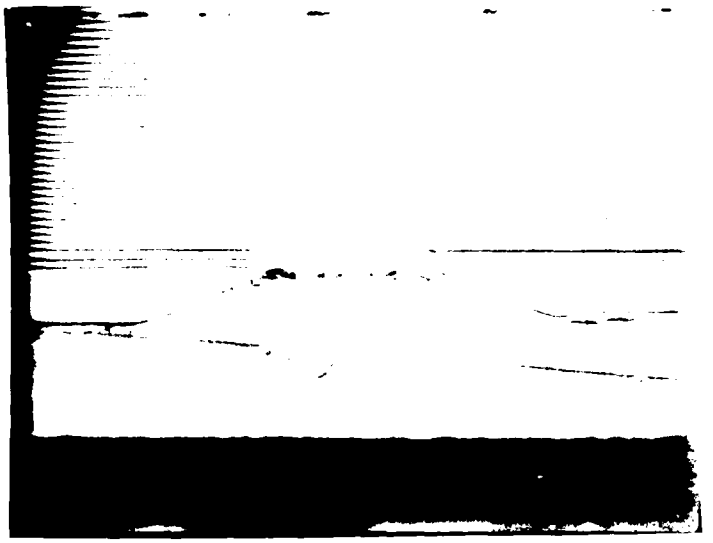


Figure 3a. An SEM Picture at 100X Showing Groove Structure of Vertical Junction Cell.

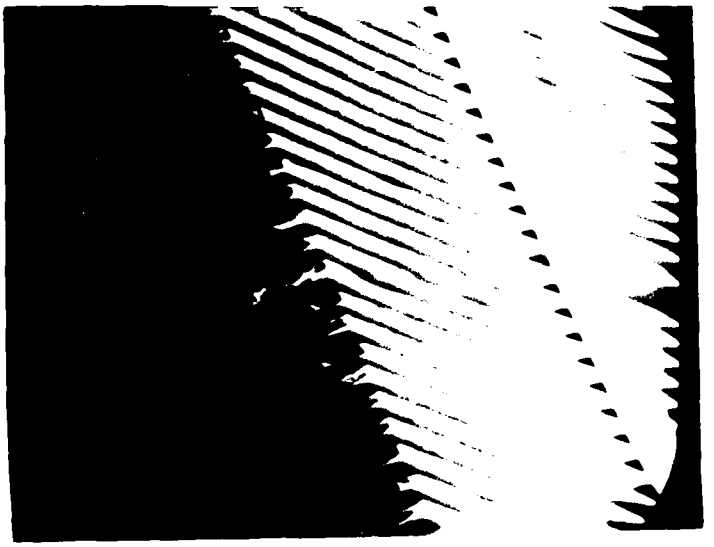


Figure 3b. An SEM Picture at 250X Showing Groove Structure of Vertical Junction Cell.

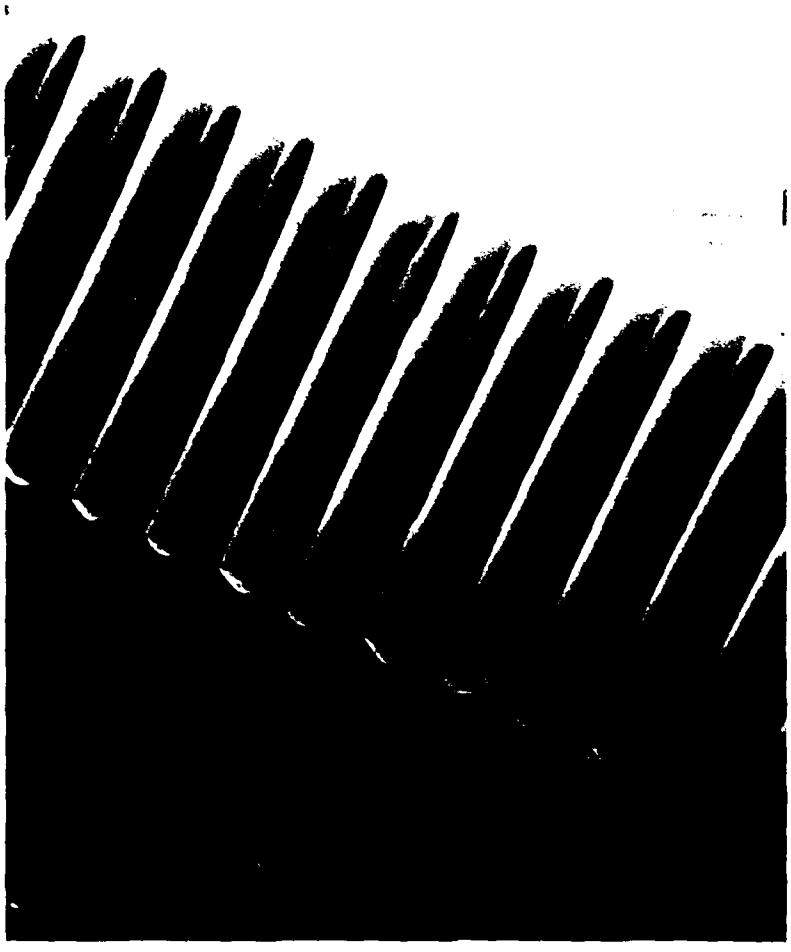
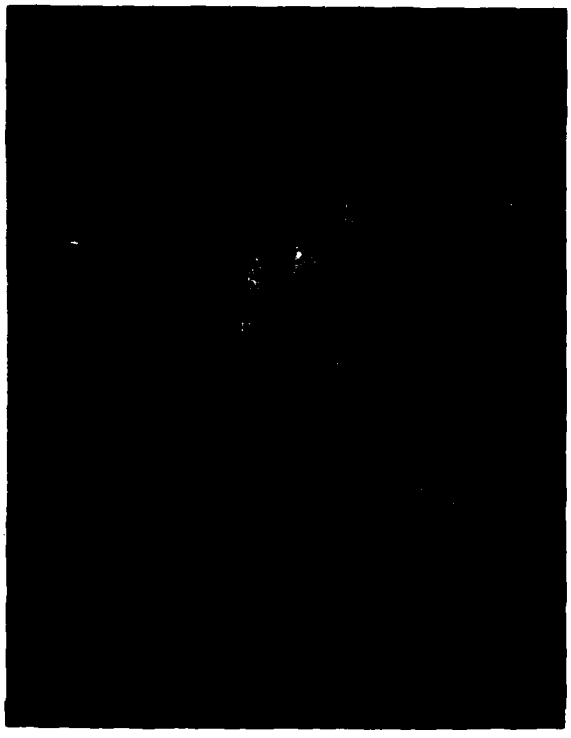
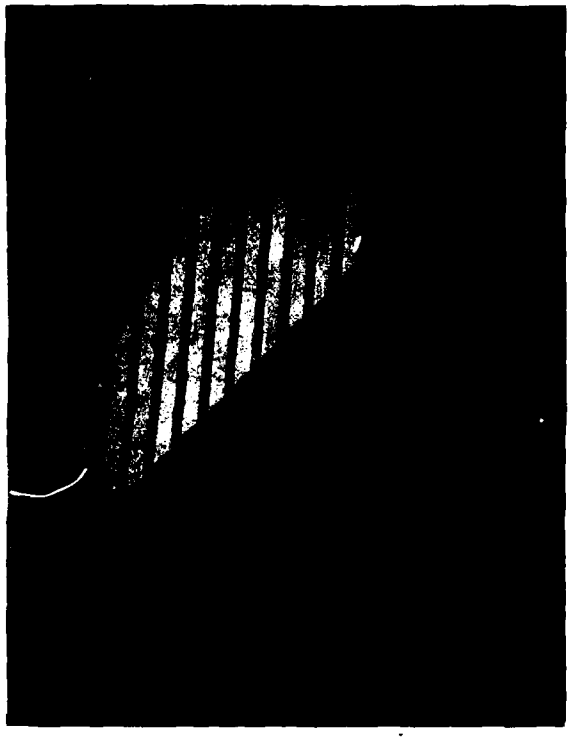


Figure 5a. An SEM Picture at 500X of a Vertical Junction Cell Broken Perpendicular to the Grooves.



Sample #C
Magnification: 720X

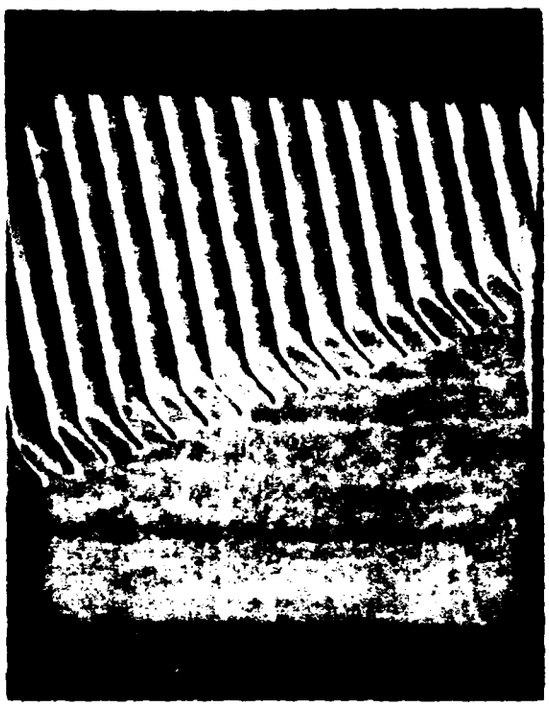


Sample #C
Magnification: 360X

Figure 4a.
No Texture Etch

Figure 4. SEM Pictures of Wall Rounding

Sample #60
Magnification: 720X



Sample #60
Magnification: 360X

Figure 4b.

After Texture Etch

Figure 4. Concluded

(a) Diffusion

The phosphorus diffusion is performed in a quartz diffusion tube using phosphine gas as the dopant source. The optimum diffusion temperature is between 840-860°C for a time period of 12-16 minutes. The sheet resistance of the diffused wafers is monitored as a close indicator of diffusion quality. Good cells result when the average sheet resistance measures between 80-100 ohm/square. Figure 5 shows continuity of junction over grooves.

(b) Back surface field formation

One important refinement in cell processing is the use of aluminum ink for the formation of the back surface field. This technique results in a higher open-circuit voltage and improved long-wavelength response compared to the previous method of vacuum-deposited aluminum. Both commercially available and Solarex-developed inks have proved successful, and most vertical junction cells have been fabricated using Englehard ink #A-3484. The paste is silk-screened onto the back of the wafers, then cured at 150°C in air. Alloying the aluminum takes place in a quartz tube in ambient air, at temperatures of 840-860°C for a relatively short time, less than one minute. The wafers are then etched in HCl (concentrated) to remove ash and unreacted aluminum.

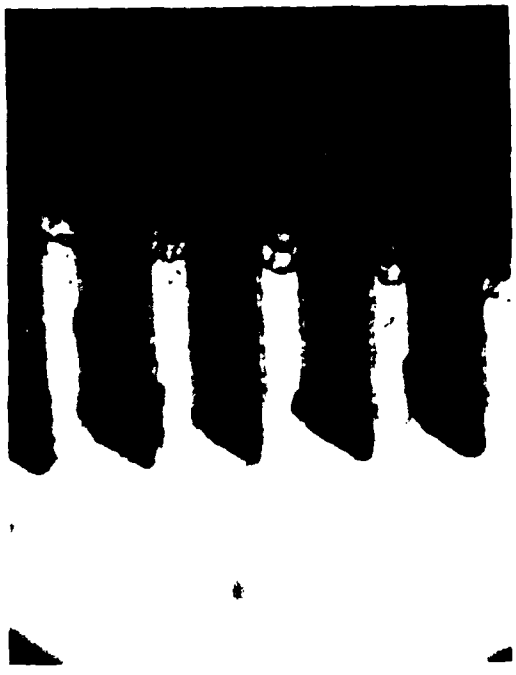


Figure 5. The Diffused Region Follows Vertical Junction Structure and is Highlighted by Copper Plating.

(c) Front contact formation

One significant advance in processing occurred when a photolithographic technique was developed which made it possible to directly evaporate the desired contact metals onto the wafer without using a shadow mask. In this way, three problem areas were eliminated: (1) surface damage to the grooved wafer by the metal shadow mask; (2) mechanical alignment of the wafer in the shadow mask, which was replaced by the superior standard mask-alignment method; and (3) overspray of metals which resulted in enlargement of the contact pattern and direct contact of palladium with the wafer surface.

This technique employs a very viscous photoresist, Hunt #206, in conjunction with multiple spin-applications and bake periods, to effectively cover all the walls of the grooved wafer. Exposure is accomplished after aligning the wafer with the desired contact pattern (Figure 6), using a standard mask aligner. After development, the wafer receives the standard titanium vacuum evaporation.

The excess resist and metals are lifted off by an acetone bath, with the titanium/palladium metals remaining only in the desired contact pattern area. Perhaps the greatest benefit resulting from this technique is its superior resolution and the freedom from accidental misalignment of the

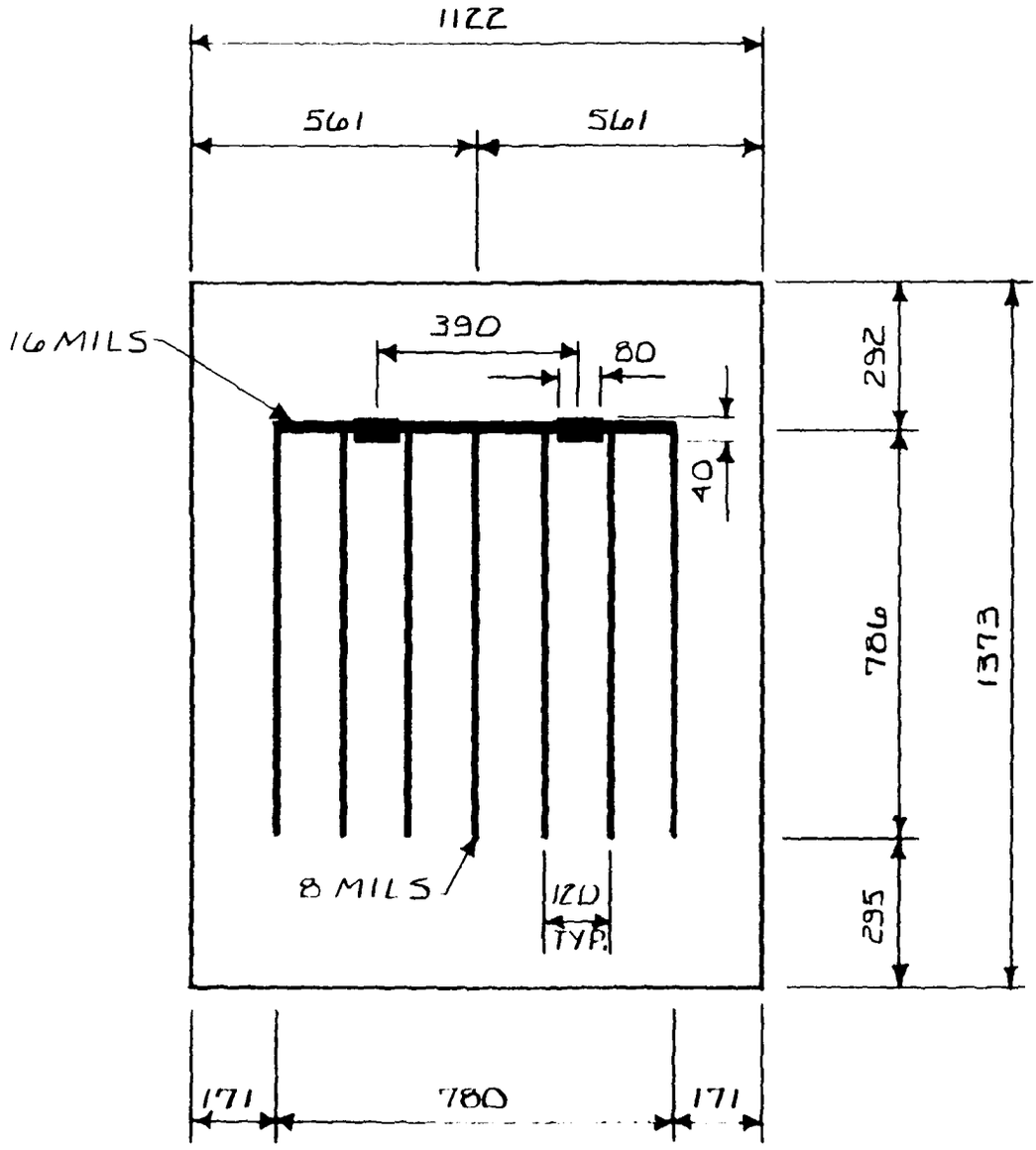


Figure 6. VJ Front Metal Contact Mask

ALL VALUES IN MILS
NOT TO SCALE

shadow mask. Cells processed in this way have achieved greater than 15.5% efficiency at AM0.

(d) Back contact formation/back surface reflector

The back metal contact is formed by vacuum evaporation of titanium and palladium. One experimental technique to improve cell current levels was the addition of a reflective surface on the back of the cells. A back surface reflector of evaporated aluminum has experimentally been found to increase the current levels in the cells, and has been included in most cell processing.

A second technique was developed to accomplish the same purpose. This technique involved the use of a standard photolithographic method to generate a grid pattern on the back of cells, so that the back contact is essentially a mesh of fine lines like the front rather than solid metal. The current gain which results may be the consequence of reduced back surface recombination and/or increased back surface reflectance.

The final step in metallization is silver electroplating with the optimal silver layer of 8-10 microns.

(e) High-temperature contact formation

One goal of this program is the development of a metallization system which could withstand 600°C for a period of several minutes.

Two different metal systems have been investigated as alternatives to the standard TiPdAg system, with promising results. In both cases, the photolithography technique described earlier was used to generate the front contact pattern onto each wafer.

One system consists of a thin layer of tantalum metal of approximately 200-300Å, evaporated by e-beam, followed by filament-evaporated chrome and gold (Ta/Cr/Au). The back of the wafers received the same treatment, followed by a thin layer (approximately 5 microns) of electroplated gold to complete the metallization. Cells fabricated with this metal system showed relatively small performance loss after one minute at 600°C.

The second system is analogous to the first except it utilizes molybdenum/chrome/gold followed by gold electroplate. Results of this experiment were equally promising but verification runs have yielded uncertain results.

(f) AR Coatings and surface treatments

Numerous anti-reflective coatings have been tried on VJ cells, including e-beam evaporated Ta_2O_5, TiO_x, and double layers of optically matched material including Ta_2O_5/Al_2O_3, Ta_2O_5/MgF_2, TiO_x/MgF_2. The most efficient uncovered cells to date have utilized a TiO_x/MgF_2 double layer AR coating. Several materials which have yielded less satisfactory results include ZnS, $PbMoO_4$, and $LiNbO_x$.

In separate experiments, SiO_2 and SnO_2 were evaporated onto the cell surface in order to increase the open-circuit voltage by passivating the surface. In each case, high series resistance resulted.

(4) Coversliding

Ceria-doped glass coverslides have been employed for all coversliding experiments. The conventional Dow Corning silicone adhesives have been used to affix the coverslides to the cells. This method of attachment has produced effective mechanical adhesion and such covered cells have successfully passed humidity testing. When coverslides were affixed to VJ cells having 3-mil deep grooves, the assemblies could not withstand thermal cycling (Ref. NTS-II, Solarex & AFWAL in-house testing). Cell assemblies using 0.5 mil grooves and 1.0 mil grooves show considerably more resistance to thermal cycling, and both categories have

successfully withstood as many as 10 cycles of (LN_2 → Room Temperature → boiling H_2O) without a change in performance (Figure 7).

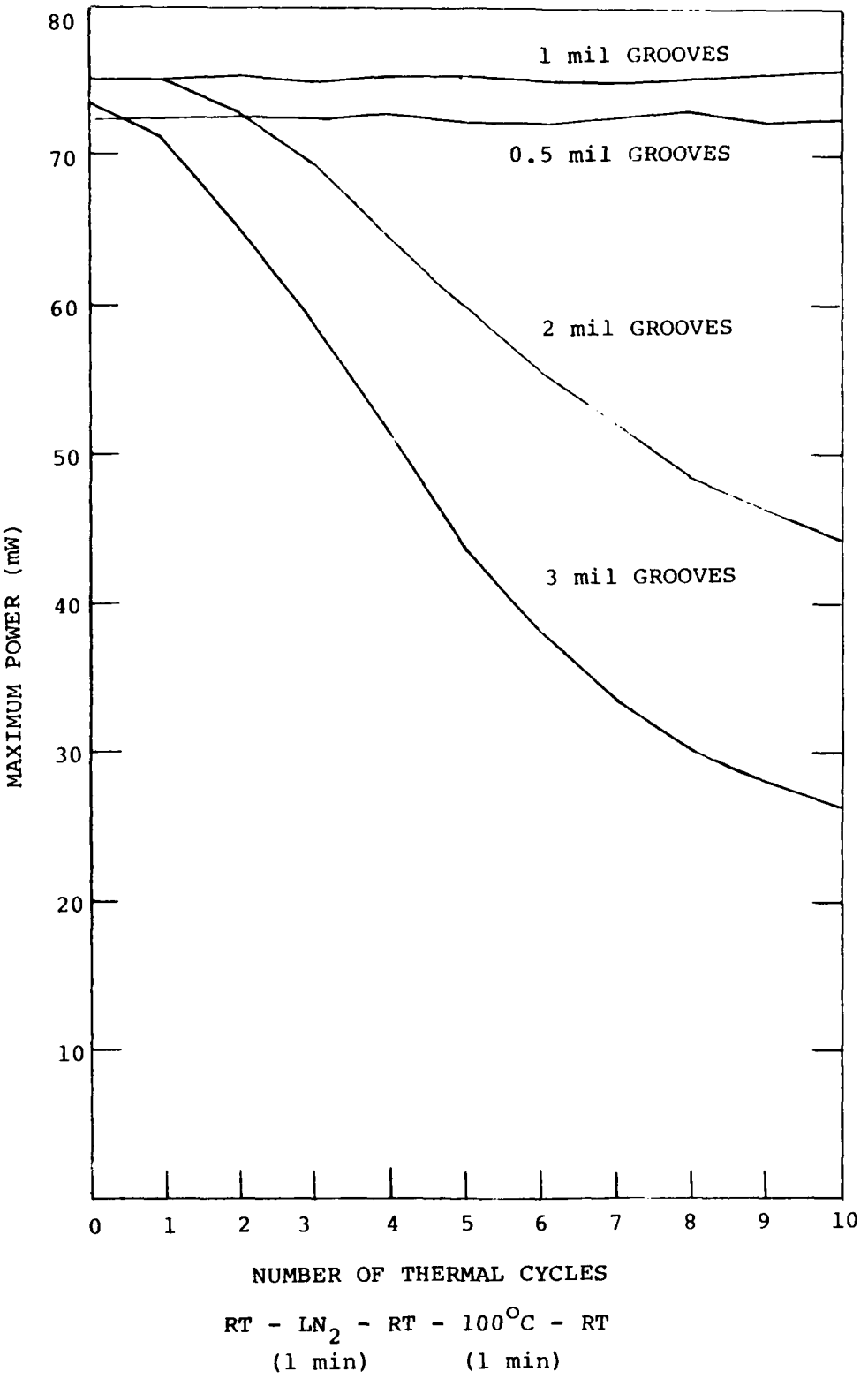


Figure 7. Thermal Cycle Tolerance of Coverslided VJ Cells

SECTION 3

DEVICE PERFORMANCE

Vertical junction solar cells have been fabricated with AM0 efficiencies in excess of 15%. Several different structures have been utilized to reach this power level. Table 1 summarizes the materials and structural parameters of the cells that have achieved the 15% efficiency level.

TABLE 1

PARAMETERS OF 15%-EFFICIENT VJ CELLS

Base Silicon:	P Type, Boron Doped
	110 Orientation
	CZ Growth
	10 to 12 Mils Thick
	2 Ω-cm Resistivity
Processing:	Gaseous Phosphorus Diffusion
	Al Paste BSF
	Ti-Pd-Ag Front and Back
	TiO_2 - MgF_2 Ar Coating
	With and without back surface reflector
Geometry:	17.5 Microns Step and Repeat
	2.5-Micron Oxide Window
	$\approx$5.0-Micron-Wide Grooves
	25- and 75-Micron-Deep Grooves
	Cells 2 cm x 2 cm area

The I-V characteristics of these cells, including a discussion of the dependence of cell performance on various geometries, structures, and parameters are described in Section 3.1. Section 3.2 discusses the use of a back surface reflector, as well as experiments with gridded backs. Section 3.3 discusses the results of a variety of AR coating experiments. Section 3.4 details the results of radiation testing. Section 3.5 discusses thermal annealing and Section 3.6 describes the optical characteristics of these cells. Finally, Section 3.7 deals with the subject of high-temperature contacts for solar cells.

1. I-V CHARACTERISTICS

The performance parameters of two 15%-efficient VJ cells using two differing geometries are given in Table 2. From these values, several important observations can be made:

- The high current densities show that there is excellent light coupling into these VJ cells. As predicted by the modeling, deeper grooves result in higher currents.

- The open-circuit voltages for VJ cells are somewhat lower than can be obtained for similarly processed planar 2 Ω-cm silicon cells, which typically exhibited open-circuit voltages in the range of 610 to 620 mV. As one would expect from their larger junction area, the deeper-grooved cells have a lower voltage than the shallow-grooved cells.

TABLE 2

PERFORMANCE OF 15% EFFICIENT VJ CELLS AT AM0 AND 25°C

I_{sc} (mA)	V_{oc} (mV)	P_{max} (mW)	Eff. (%)	Corning #9788 I_{sc} Blue (mA)	Corning #2408 I_{sc} Red (mA)	Fill Factor (%)
25 micron groove depth, without BSR						
175	597	82	15.1	48	91	78.5
75 micron groove depth, without BSR						
177	583	82	15.1	49	92	79.5
25 micron groove depth, with BSR						
174	602	82	15.1	46	94	78.3
		└(84 mW after 90 sec sinter)				
25 micron groove depth, with BSR VERIFICATION LOT, 85 SEC SINTER						
178	590	84	15.5	45	97	79.9

- The fill factors are comparable with other high-efficiency silicon solar cells, showing that the metallization design is adequate.

Using the thinning technique reported in Section 2, VJ cells on substrates as thin as 75 microns have been fabricated. Table 3 lists the maximum power obtainable to date for a variety of substrate thicknesses.

TABLE 3

THIN-SUBSTRATE VJ CELLS

Best Performance for 2 cm x 2 cm Cells

Thickness of Silicon (Microns)	P_{max} (mW) at AM0
275	84
175	80
125	78
75	74

To compare the effects of groove depth, substrate thickness and bulk resistivity, an experiment was conducted. Using identical processing, cells were fabricated of 2 Ω-cm and 10 Ω-cm silicon using 250-micron and 175-micron-thick wafers and etching 25-, 50- and 75-micron-deep grooves. The results are shown in Table 4. The following observations can be made:

- Short-circuit current is nearly insensitive to bulk resistivity.
- Short-circuit current decreases with decreasing substrate thickness.
- Open-circuit voltage decreases with increasing bulk resistivity.
- Open-circuit voltage is unaffected by substrate thickness.
- Open-circuit voltage decreases with increasing groove depth.

TABLE 4

COMPARISON OF ELECTRICAL PERFORMANCE

Thickness	Resist. (ohm-cm)	Groove Depth→ (Microns)	$\bar{I}_{sc}$ (mA)			$\bar{V}_{oc}$ (mV)			$\bar{P}_{max}$ (mW)		
			25	50	75	25	50	75	25	50	75
250 Microns	2		173	172	175	596	586	577	81	79	78
	10		172	172	173	585	576	572	78	78	77
175 Microns	2			158	168		585	578		74	75
	10		164	168	165	578	574	565	73	74	72

2. BSR AND GRIDDED BACKS

In silicon, as the photon energy of light goes to lower values the absorption depth increases. Consequently, there is a range of light energy in the infrared region that is sufficient to generate carriers but has an absorption depth on the same order as the wafer thickness. The number of carriers generated by light in this range can be approximately doubled by use of a back surface reflector (BSR) to double the path length.

Cells with both a back surface field and a back surface reflector have been fabricated. The back surface field is formed by aluminum paste alloy. After alloy the backs are cleaned in hydrochloric acid. For a cell without a back surface reflector the next step would be to evaporate titanium and palladium. In order to form a back surface reflector a layer of aluminum is vacuum evaporated, followed by a titanium and palladium evaporation.

The average electrical performance for a non-BSR lot and two BSR lots are shown in Table 5. In all cases the cells were about 275 microns thick and had a 25 micron groove depth.

TABLE 5

COMPARISON OF NON-BSR AND BSR LOTS

Lot	Type	Average I_{sc}	Average V_{oc}	Average P_{max}
#16	Non-BSR	173	595.5	81.
#21	BSR	174	600.	80.5
#24	BSR	177	591.	82.

The lots shown in Table 5 were chosen to represent the best that each process has achieved. The BSR may be responsible for the particularly high average current in Lot #24.

In a set of experiments, gridded backs were compared to solid titanium backs. It is possible that during the contact sintering step the titanium that diffuses into the back increases the back surface recombination. This effect can be reduced by using a gridded contact so that most of the back is bare silicon (with a back surface field).

For the gridded back experiments the back surface field was formed by aluminum paste alloy. The back was then cleaned in hydrochloric acid. No back surface reflector was used. The solid backs had the usual Ti/Pd/Ag contacts. The gridded backs used the same metallization but with a pattern formed photolithographically.

The experimental results, shown in Table 6, indicate that cell performance can be improved using a gridded back. The cells had 25 micron grooves, double layer AR coating and were of 2 ohm-cm resistivity. However, the peak power was not as high as back surface reflector cells.

Aside from back surface recombination effects, gridded backs may show more current than solid Ti backs because internal reflection from the bare silicon may be greater than the sintered Ti/Si interface.

TABLE 6

AVERAGE ELECTRICAL PERFORMANCE FOR GRIDDED AND SOLID BACKS FOR THREE WAFER THICKNESSES

	Wafer Thickness (mils)	I_{sc} (mA)	V_{oc} (mV)	P_{max} (mW)
Gridded	10 - 12	174.8	589.8	79.5
Solid	10 - 12	170.	590.	77.5
Gridded	5	171.5	587.	76.5
Solid	5	166.5	586.	77.
Gridded	3	166.2	577.	71.5
Solid	3	155.	583.	68.

3. AR COATINGS

A variety of antireflective coatings have been employed on VJ cells. The evaporated layers are applied perpendicular to the surface (as for a planar cell) and the current increase is consistent with that expected as a result of the increase in absorption of the planar areas. The liquid AR coating results in a thicker coating on the walls and improves the current collected for non-perpendicular illumination. The following subsections describe the various AR coating results.

a. Single-Layer Vacuum-Evaporated Ta_2O_5

This is the standard space-quality quarter-wavelength AR coating, with an index of refraction of 2.05 to 2.2. The amount of current increase depends upon the geometry of the VJ cell and is consistent with the presence of this AR coating on the planar areas, and with 100% absorption of light that enters the grooves. With this AR coating there is still a minimum current loss of 6.1% due to reflection. In addition, we have observed a loss of open-circuit voltage upon application of the Ta_2O_5 coating. It is believed that this is due to an increased front surface recombination velocity caused by our particular technique for deposition of the Ta_2O_5. While all early VJ cells were fabricated using a single-layer Ta_2O_5 AR coating, more recent cells have used either TiO_x single layers or multi-layer AR coatings.

b. Single-Layer Vacuum-Evaporated TiO_x

TiO_x is also a standard space-quality quarter-wavelength AR coating with an index of refraction of 2.0 to 2.2. Once again, the amount of current increase of VJ cells using it is consistent with its presence on the planar areas and with 100% absorption of light that enters the grooves. Since it is only a single-layer AR coating, there is still a minimum current loss of 6.1% due to reflection. However, there is an increase in open-circuit voltage upon application of the TiO_x. Therefore, later samples have utilized TiO_x rather than Ta_2O_5.

c. Liquid Ta_2O_5

A commercially available Ta_2O_5 liquid AR material was obtained from Allied Chemical Corporation. The liquid coatings have been applied to VJ cells by spinning, spraying and dunking. The absorption of coated cells was improved over bare cells with each of these methods, but none of the liquid AR coatings were as good as the best evaporated AR coatings. There is some evidence that the liquid AR does increase absorption in the sides of the walls, however. Figure 8 shows the short-circuit current of a VJ cell with liquid AR coating as a function of angle of incidence. As can be seen, the current is a maximum at an angle 15° from normal. Vacuum-evaporated AR coated cells have exhibited

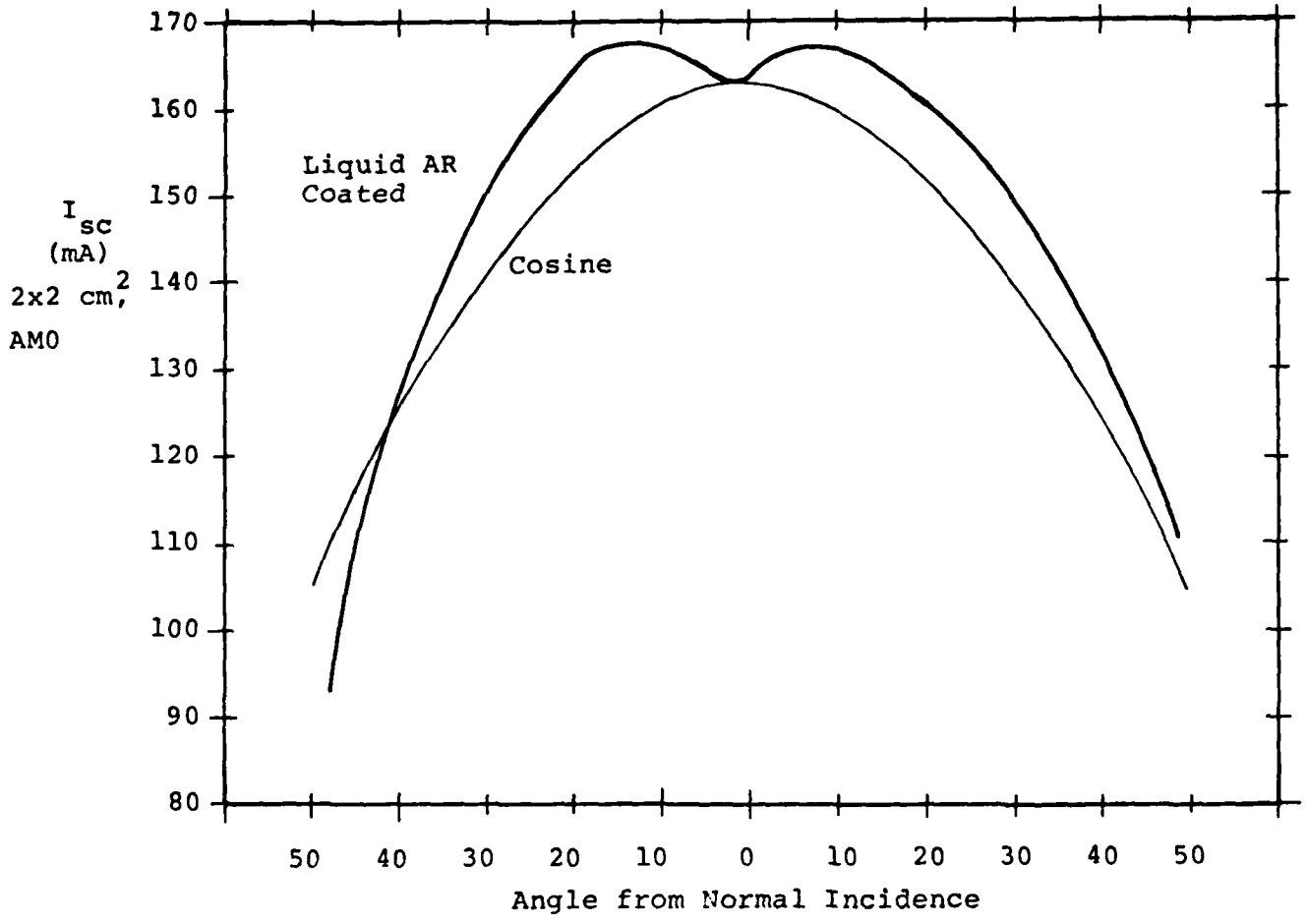


Figure 8. Angular Dependence of Short Circuit Current for Liquid AR Coatings

this phenomenon only after irradiation. It is therefore possible that the liquid AR will increase the fraction of light absorbed in the walls and therefore [illegible] the radiation resistance of the cells.

Finally, in an attempt to develop a coversliding technique for VJ cells, liquid AR material was used to fill in the grooves. The cells, however, suffered severe loss in current (Figure 9), indicating that thick layers of the AR coating are not transparent.

d. Double-Layer AR Coatings

Double-layer AR coatings can be utilized to further reduce reflection from the silicon surface. With the proper choice of materials, a double-layer AR coating can reduce reflection so that less than 2% of the potential current is lost due to reflection. Increases in current of up to 5% above single-layer-coated cells have been observed for cells using double-layers of TiO_x and MgF_2 or Ta_2O_5 and MgF_2. Figure 10 shows reflection versus wavelength for a single-layer and double-layer AR coating on a VJ cell. All of the highest efficiency cells have employed double-layer AR coatings. At present, TiO_x is the preferred bottom layer because of the voltage problems associated with Ta_2O_5.

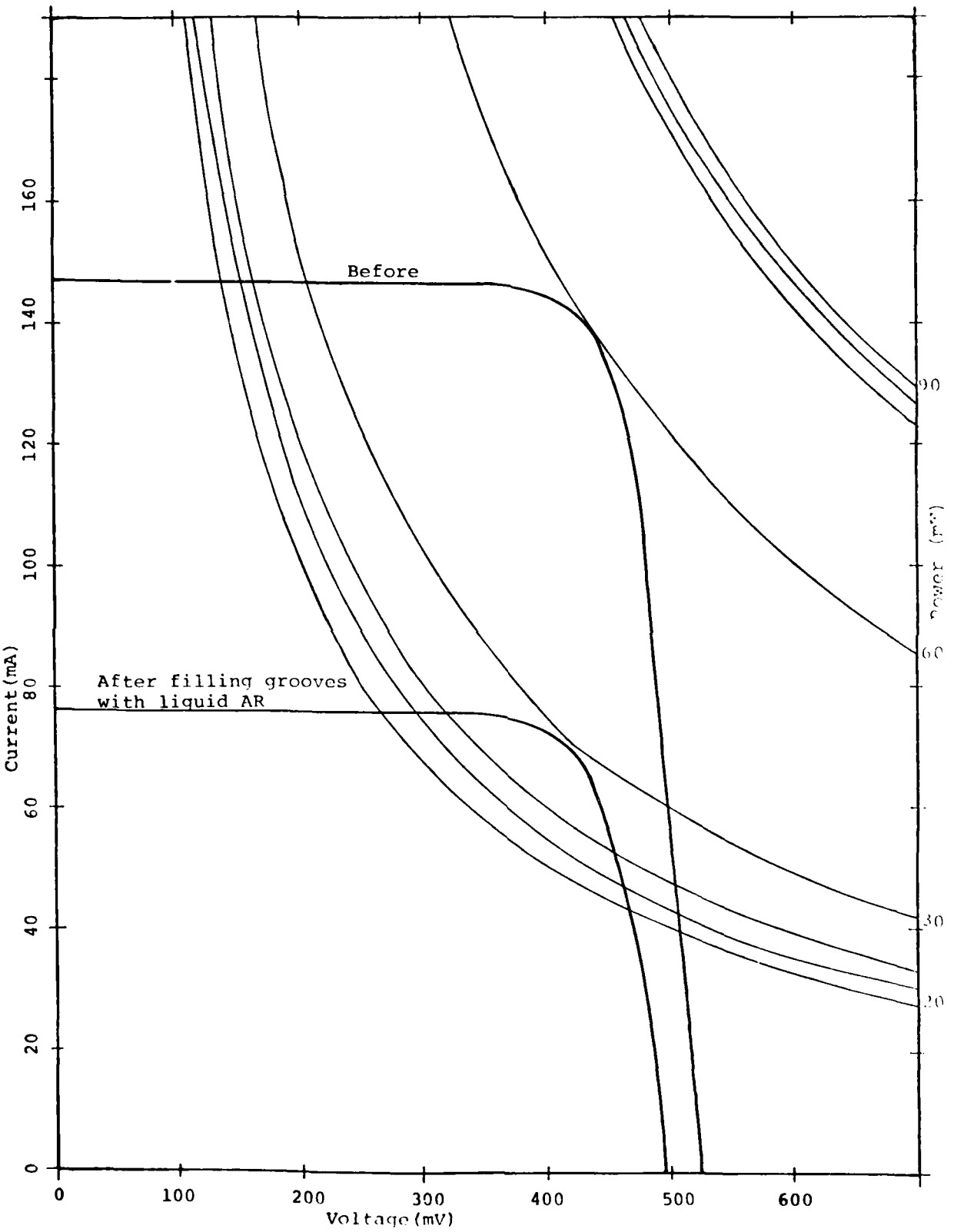


Figure 9. IV Curve Before & After Filling the Grooves with Liquid Ta_2O_5

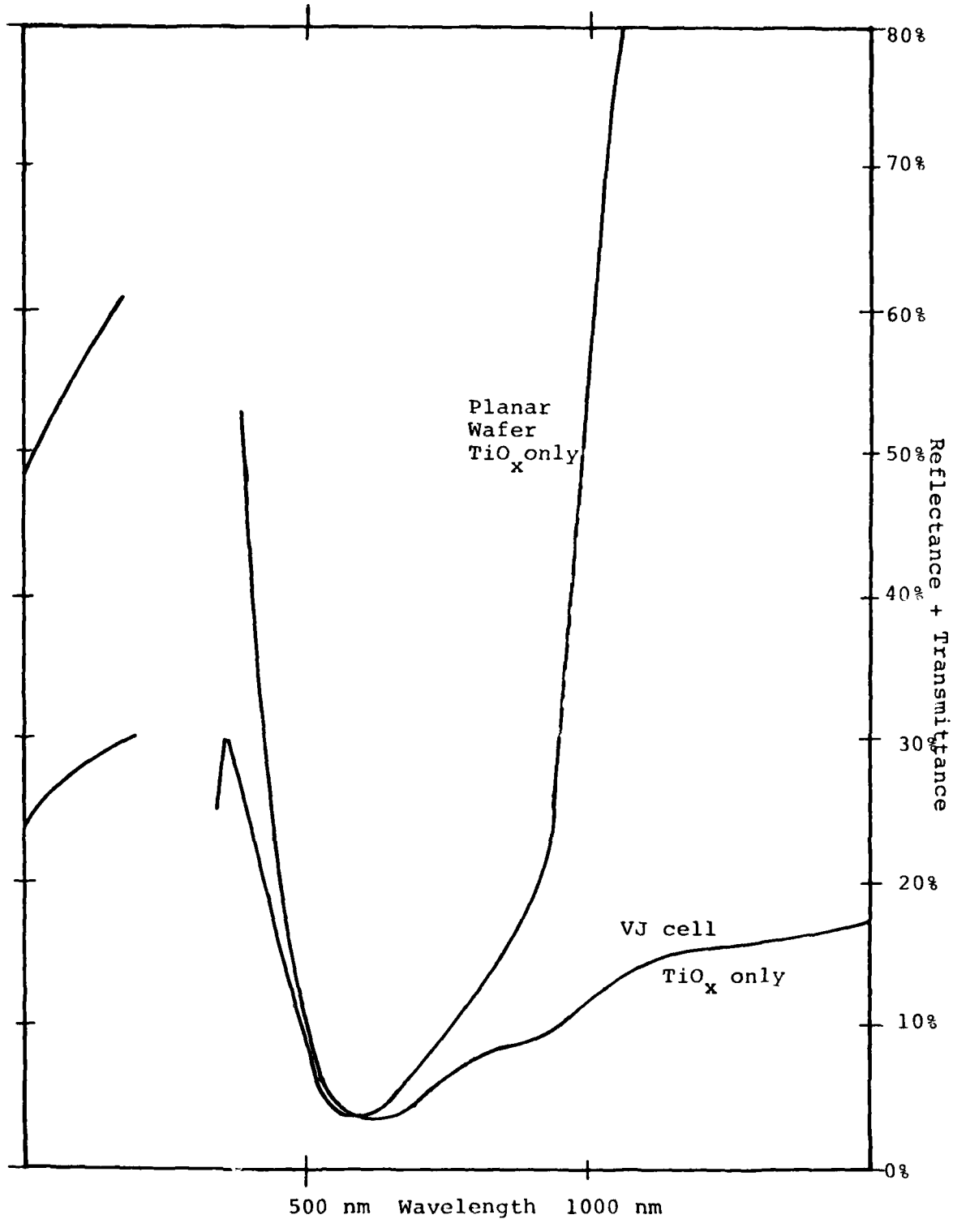


Figure 10a. Reflectance vs Wavelength for a Single Layer and Double Layer AR Coating on a VJ Cell

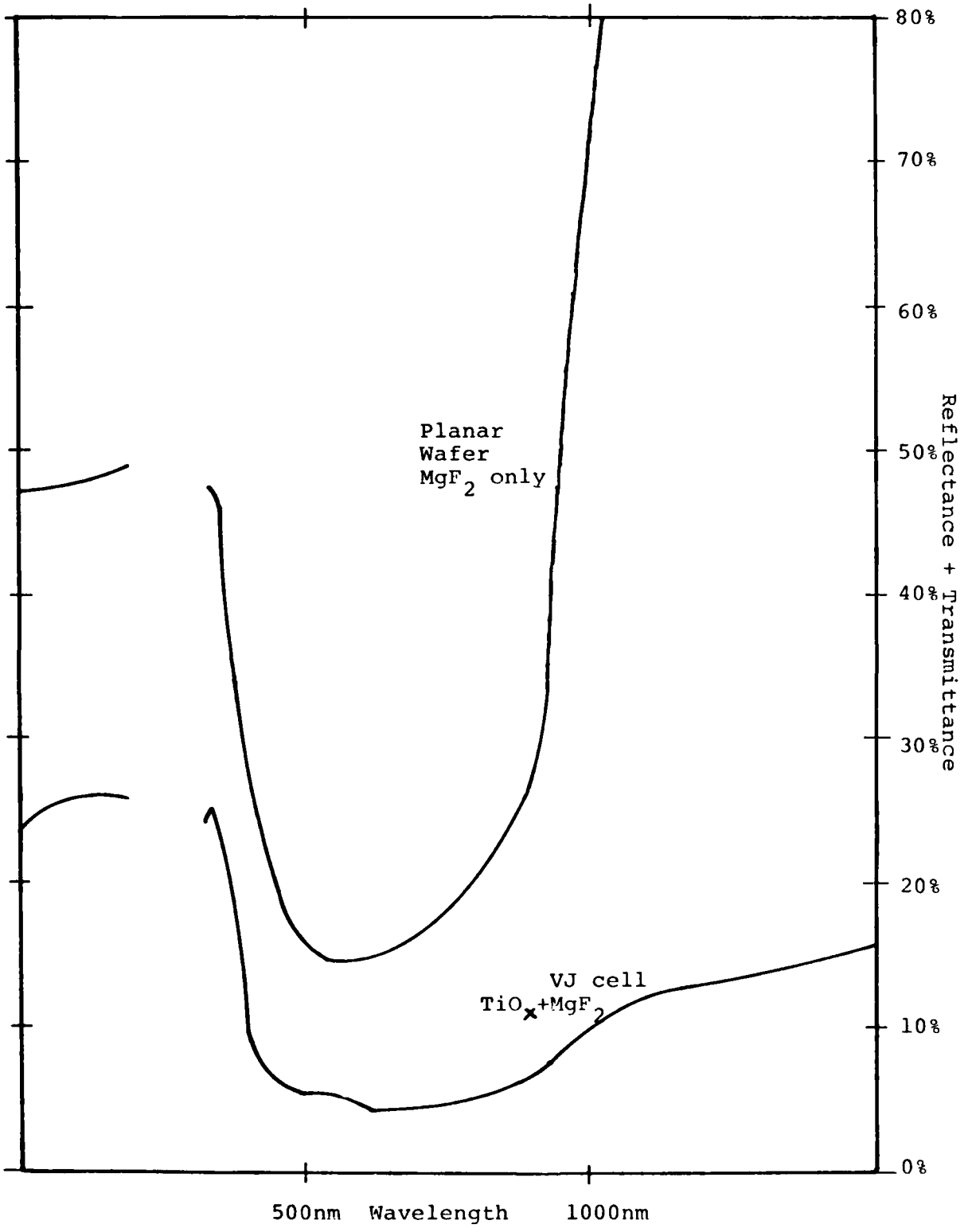


Figure 10b. Reflectance vs Wavelength for a Single Layer and Double Layer AR Coating on a VJ Cell

It should be noted that the TiO_x-MgF_2 system is being used as the best match between the silicon and air. The best match for a filtered cell would require two layers with higher index of refraction, namely 2.6 for the bottom layer and 1.7 to 1.8 for the top layer.

To obtain a high index layer (≈2.6) we have tried ZnS, $LiNbO_x$, and $PbMoO_4$, as well as TiO_2 evaporated in a partial pressure of oxygen with the substrate heated to 200°C. Electron beam evaporation was used to deposit the layers. The results are shown on Table 7.

TABLE 7

EXPERIMENTAL AR COATINGS

Material	Results
ZnS	Decomposed, uneven coating
$LiNbO_x$	Decomposed
$PbNoO_4$	Refractive index measured as 2.25
TiO_2+O_2	Refractive index measured as 2.20, same as TiO_2 without partial pressure of oxygen

While the index of evaporated $PbMoO_4$, (2.25) is slightly higher than TiO_2 (2.2) we feel that the process variability that may occur when using a ternary compound makes TiO_2 preferable.

4. RADIATION RESISTANCE

A matrix of cells underwent radiation testing. The cells consisted of 2 and 10 ohm-cm bulk resistivity; 3, 5, 7 and 11 mils wafer thickness; and 1, 2 and 3 mils groove depth. The cells were made with the 17.5 step and repeat/2.5 oxide window mask. The cells had a double layer AR coating, no coverslide, aluminum paste BSF and no back surface reflector. The irradiation was done at the Naval Research Laboratory in Washington, D.C. The cumulative dosages were $3. \times 10^{13}$, 1.2×10^{14}, $3. \times 10^{14}$, $1. \times 10^{15}$, $3. \times 10^{15}$ and $1. \times 10^{16}$ 1 MeV electrons/cm^2. The electrical measurements shown on the graphs were made using a Xenon light source calibrated to AMO. The cells were annealled for 16 hours and 60° C.

The short circuit current for wafers of 11, 7, 5, and 3 mils thickness is shown in Figures 11, 12, 13 and 14. These figures show that for a given wafer thickness the initial I_{sc} is similar for various groove depths and resistivities but that a clear trend is observed after irradiation. The trend is that 10 ohm-cm silicon is more radiation tolerant than 2 ohm-cm and that deeper grooves give higher end-of-life current.

To compare an eleven mil thick planar cell with eleven mil thick VJ cells a graph of relative current (normalized by the pre-irradiation current) is shown in Figure 15. The best VJ cell (3 mil grooves, 10 ohm-cm) can supply 40% more

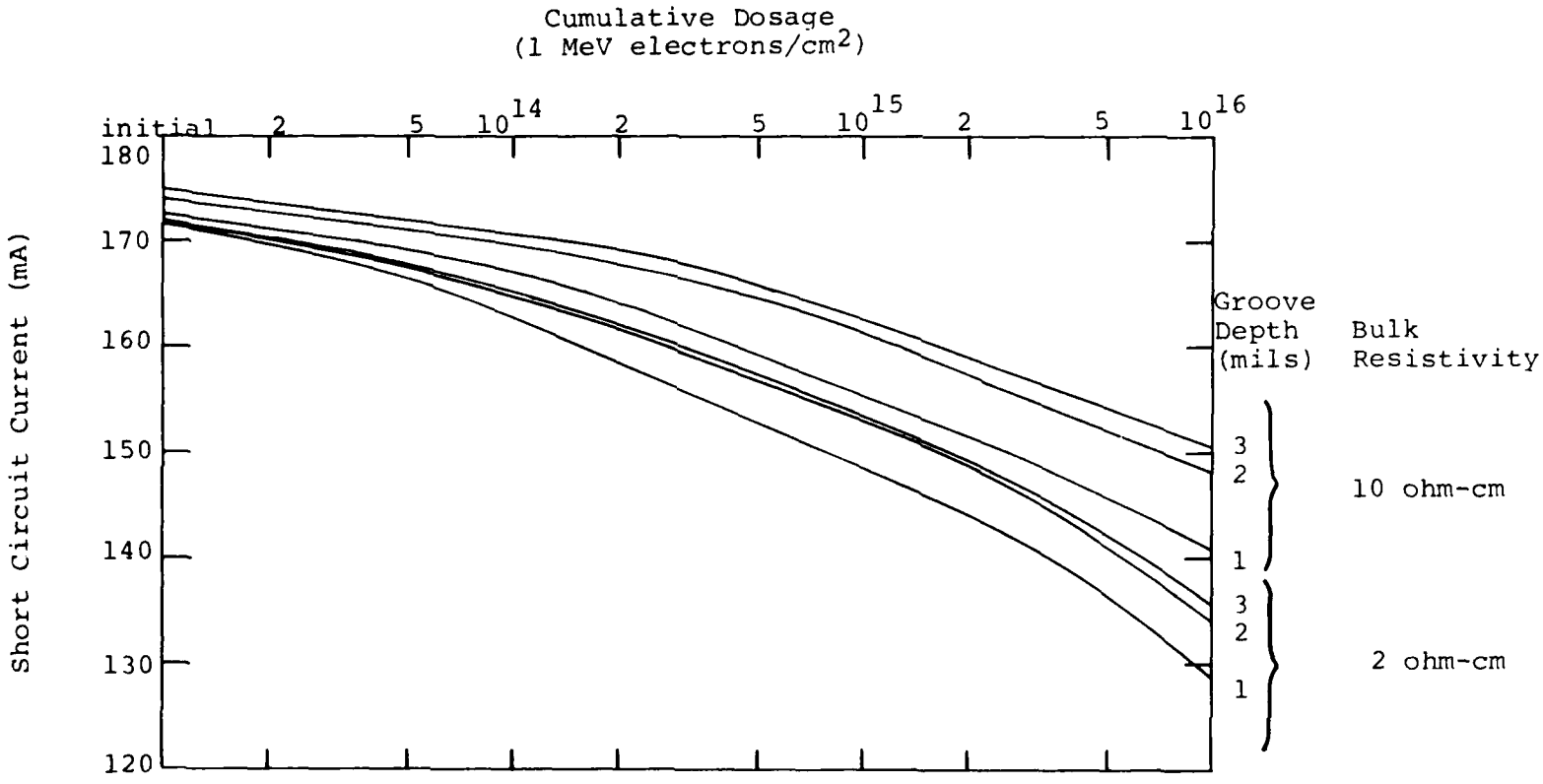


Figure 11. Short Circuit Current vs. Fluence, 2 cm x 2 cm VJ Cell, 11 mils Wafer Thickness.

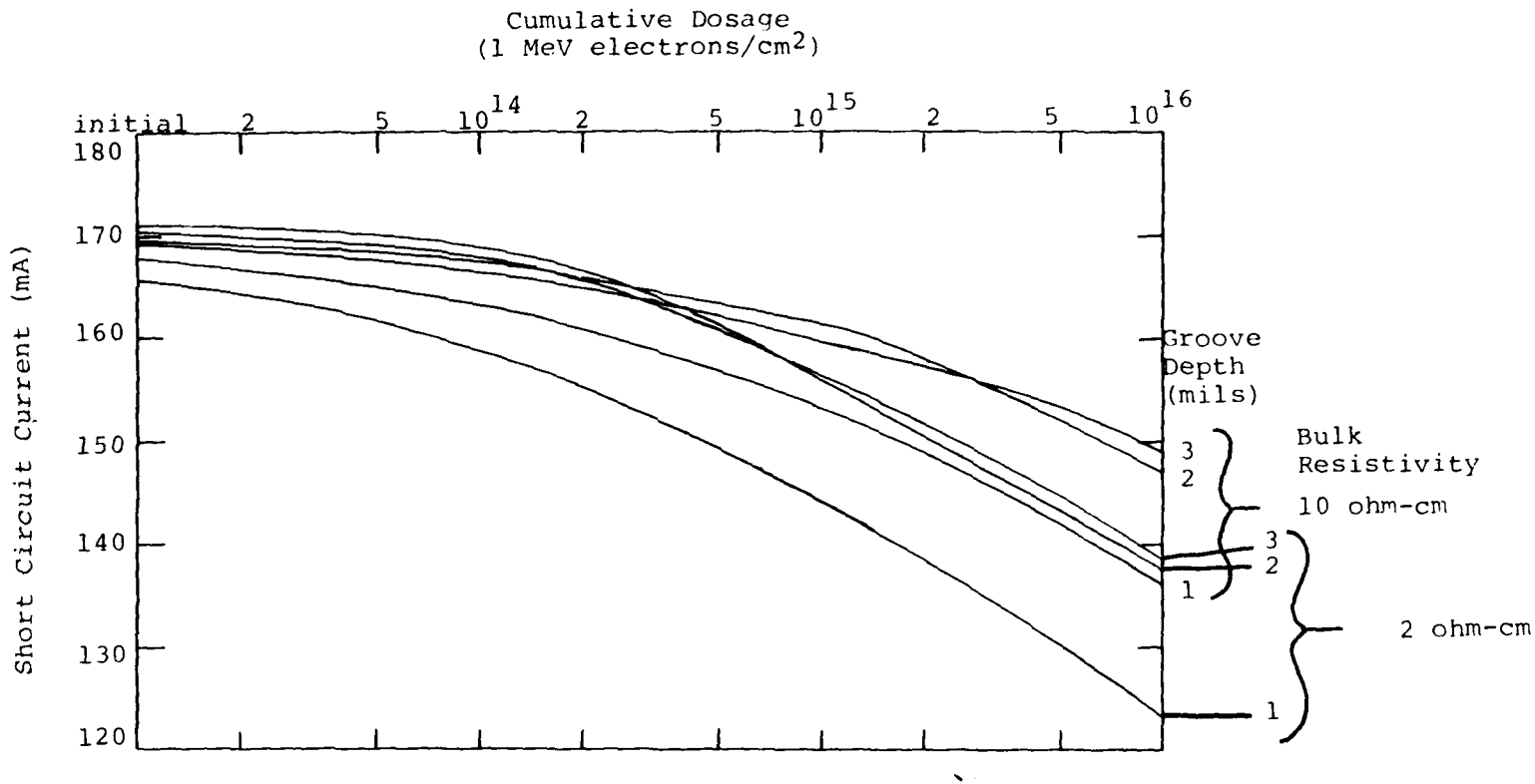


Figure 12. Short Circuit Current vs. Fluence, 2 cm x 2 cm VJ Cell, 7 mils Wafer Thickness

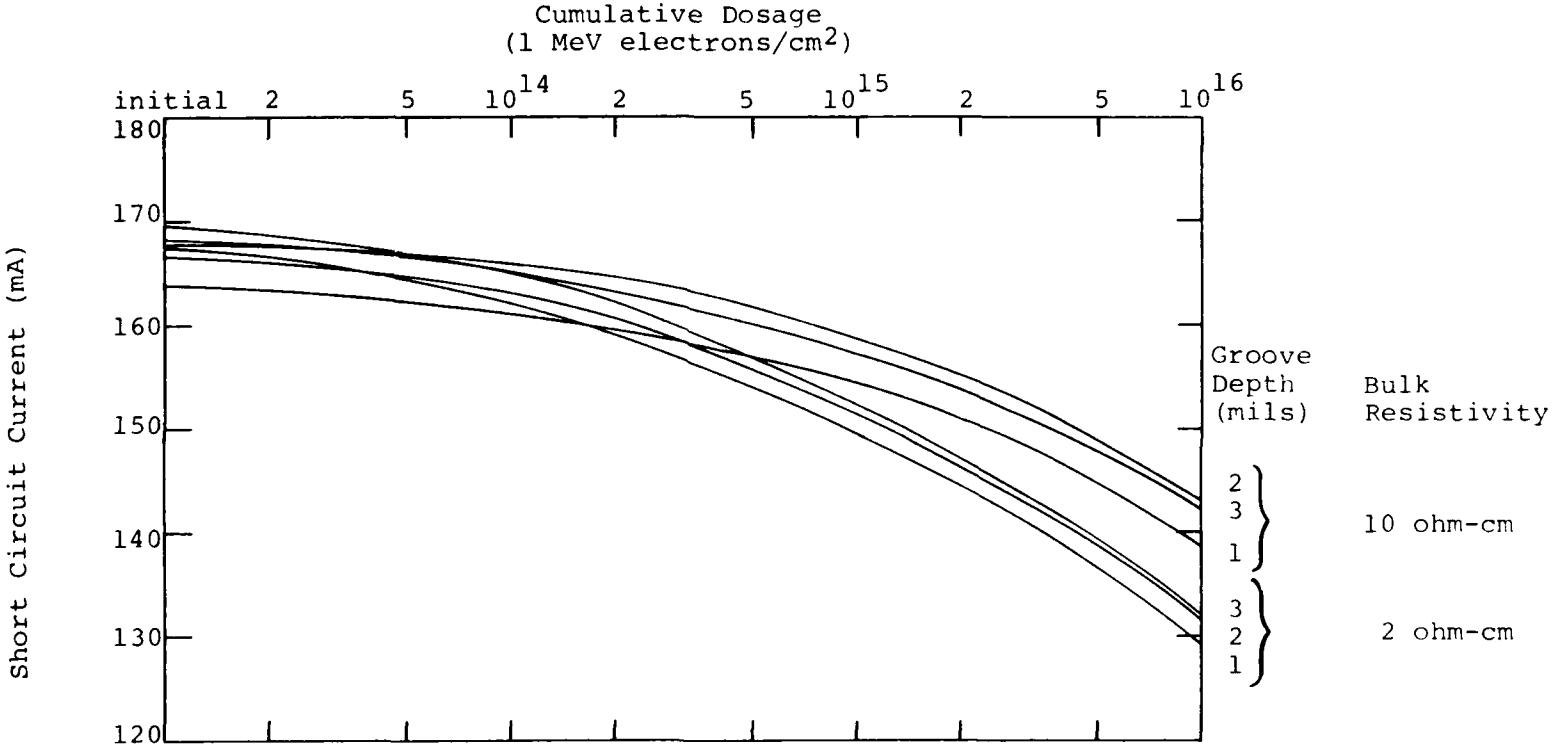


Figure 13. Short Circuit Current vs. Fluence, 2 cm x 2 cm VJ Cell, 5 mils Wafer Thickness.

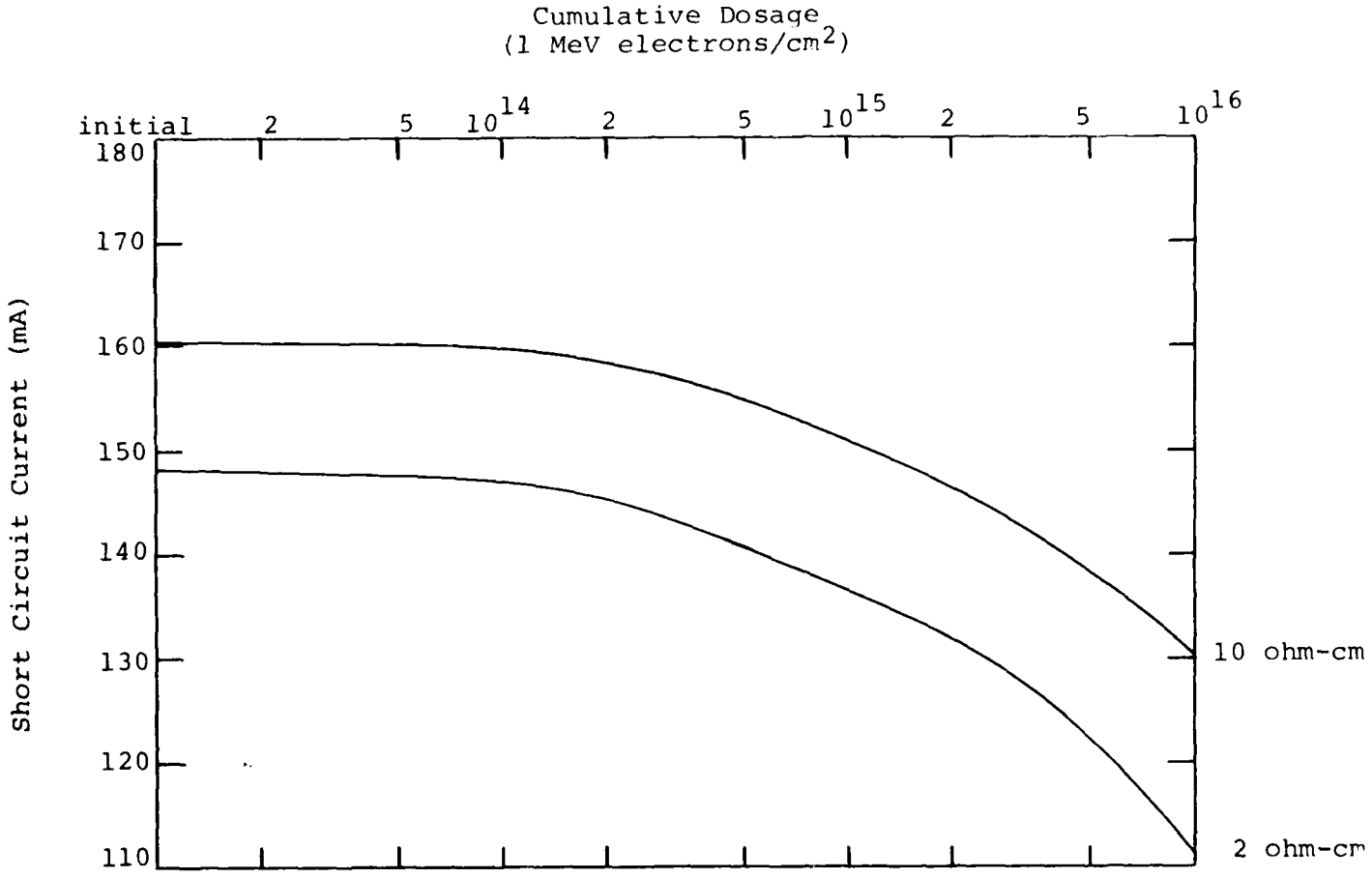


Figure 14. Short Circuit Current vs. Fluence, 2 cm x 2 cm VJ Cell, 3 mils Wafer Thickness, 1 mil Groove Depth.

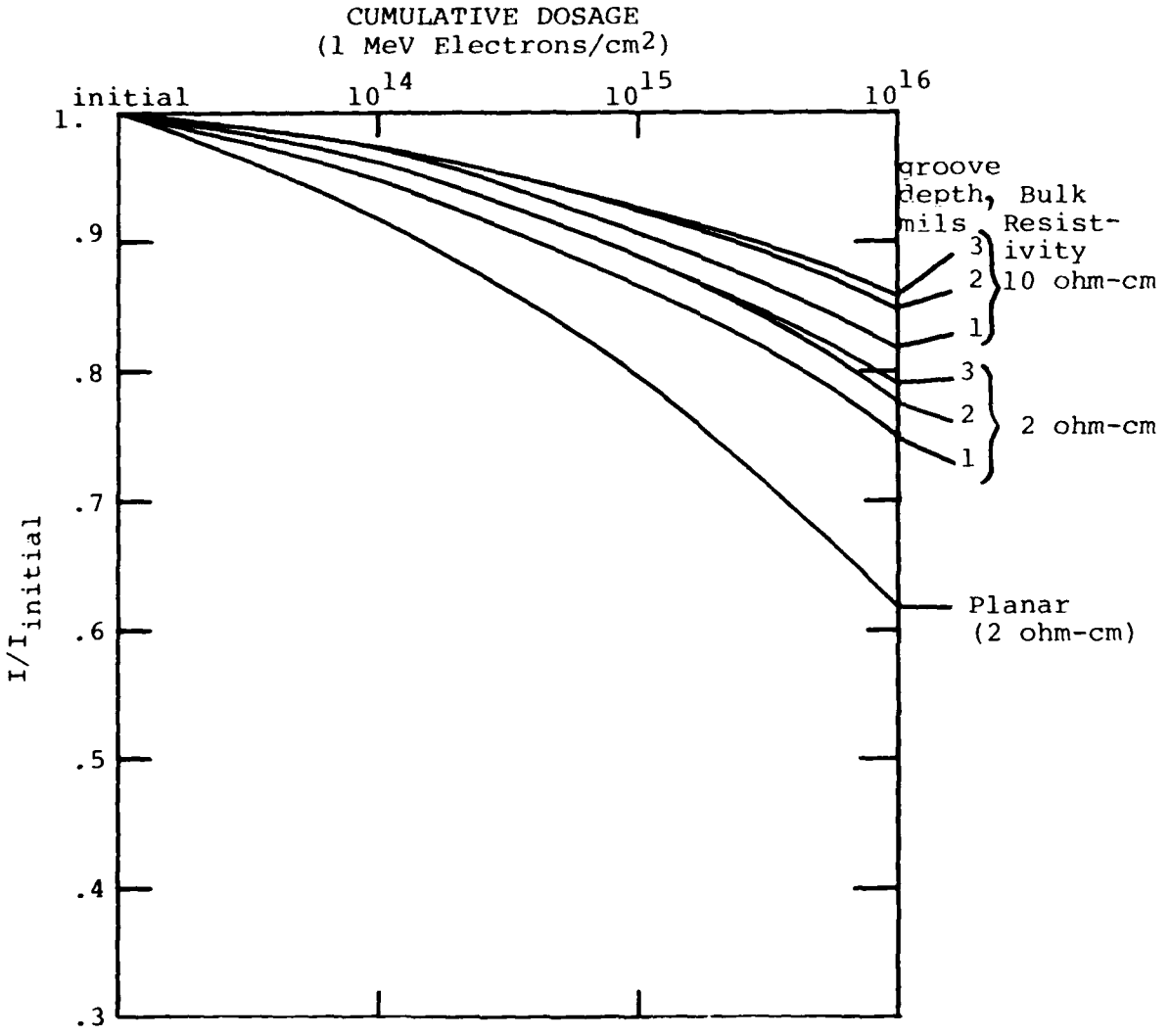


Figure 15. Relative Short Circuit Current ($I/I_{initial}$) vs. Fluence for 11 mil Thick VJ Cells and Planar Cell

short circuit current than a planar cell after a dosage of 10^{16} 1 MeV electrons/cm^2.

The variation of open circuit voltage with irradiation dosage is shown in Figure 16. The relationship between bulk resistivity and V_{OC} is the opposite of that found for current, i.e., the low resistivity material gives a higher value. The inversion also applies to groove depth, i.e., deeper grooves have a lower V_{OC}. An average planar cell is compared to VJ cells in terms of relative voltage in Figure 17.

Because of the inverted relationship between current and voltage the end-of-life power is very similar for various groove depths and bulk resistivities. The power vs fluence is shown in Figure 18. Only 7 mil thick wafers are shown because 11 and 5 mil thick wafers are very similar. Relative values of current are shown in Figure 19. Differences in end-of-life power between various groove depths and wafer thicknesses can best be seen on an expanded scale shown in Figure 20. While it can be seen that deeper grooves have better EOL power, it is important to keep in mind that the difference is only about 2% power per mil of groove depth and that the thicker substrate cells typically exhibited more power before irradiation. Figures 21 and 22 show the relative maximum power (P/P initial) vs. electron fluence as a function of substrate thickness. As can be seen in most cases, the thinner VJ cells are more radiation resistant than the thicker VJ cells. This effect is most pronounced for 2Ω-cm ultrathin 3 mil thick VJ cells with 1 mil deep grooves, which show a 13% power loss after a 10^{15} dosage of 1 Mev electrons compared

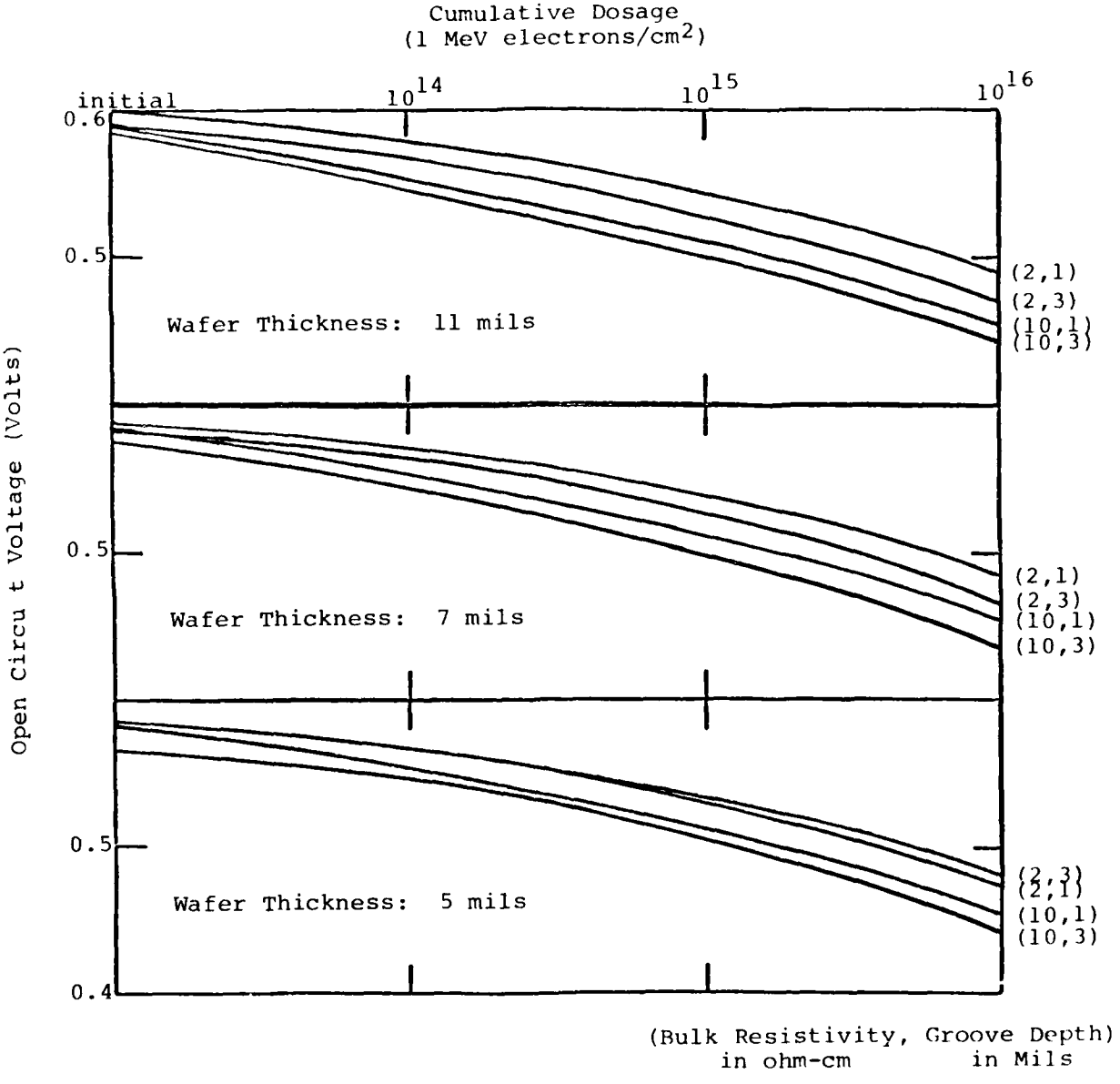


Figure 16. Open Circuit Voltage Versus Radiation Fluence.

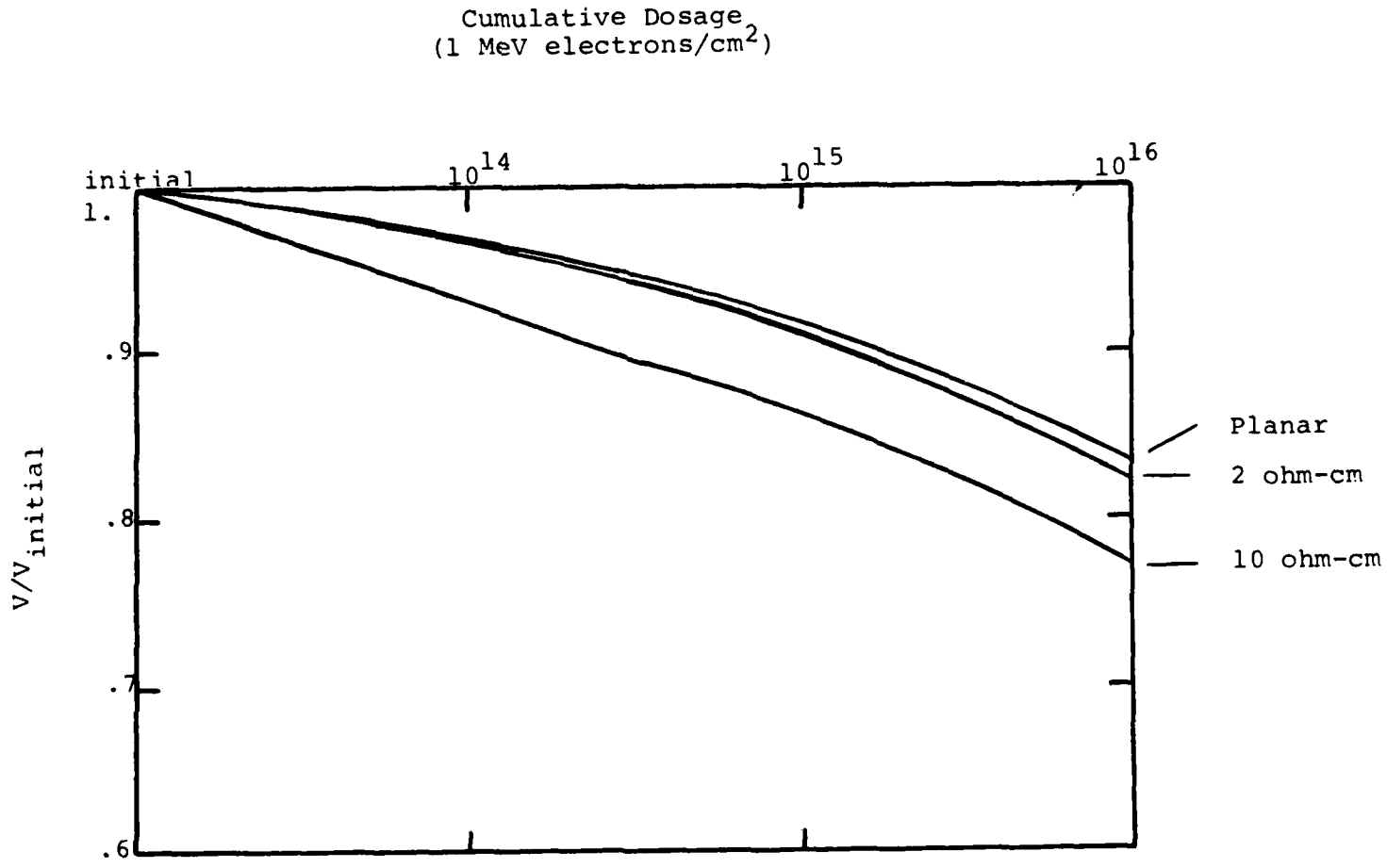


Figure 17. Relative Open Circuit Voltage ($V/V_{initial}$) vs Fluence for VJ Cells 1 mil Thick With 1 mil Deep grove and Planar Cells

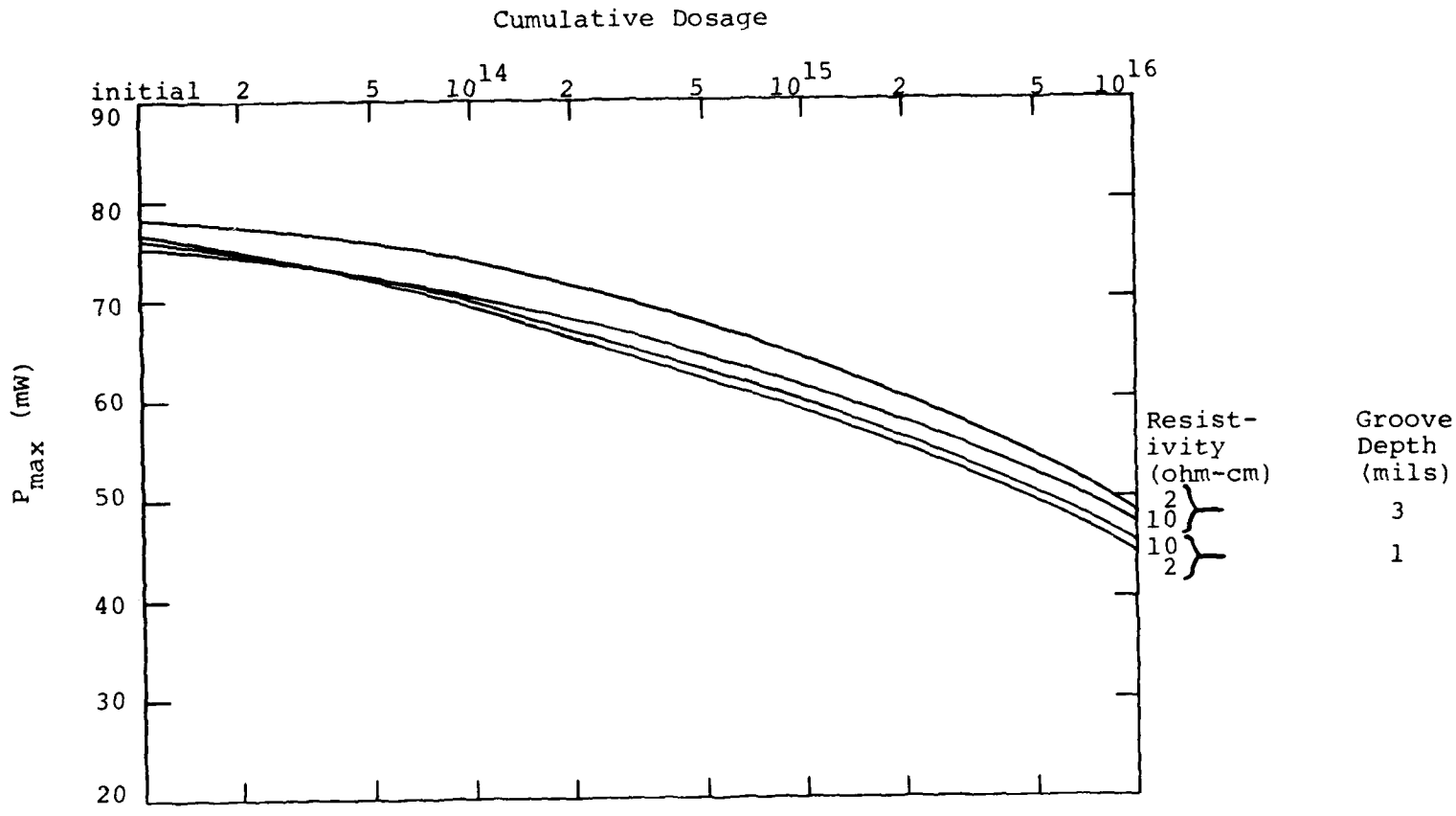


Figure 18. Maximum Power Point vs. Fluence, 2 cm x 2 cm VJ Cell, 7 mils wafer thickness.

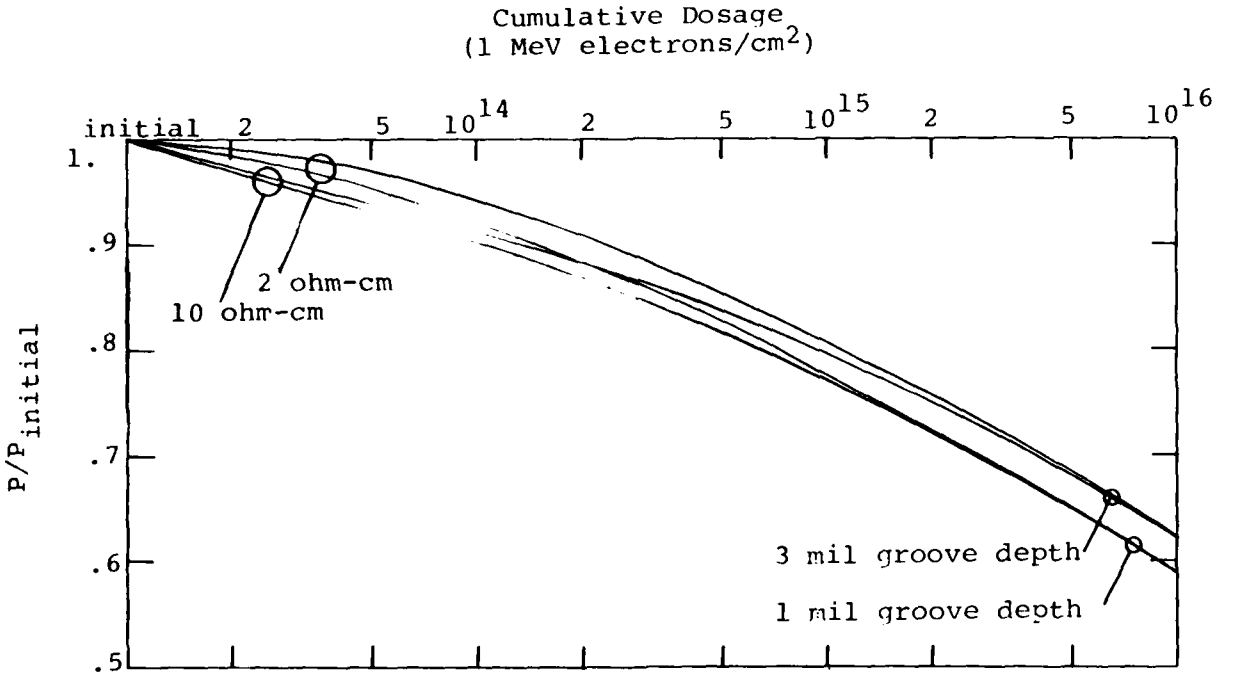


Figure 19. Relative Maximum Power Point ($P/P_{initial}$) vs. Fluence for 2 cm x 2 cm VJ Cells, 7 mils wafer thickness.

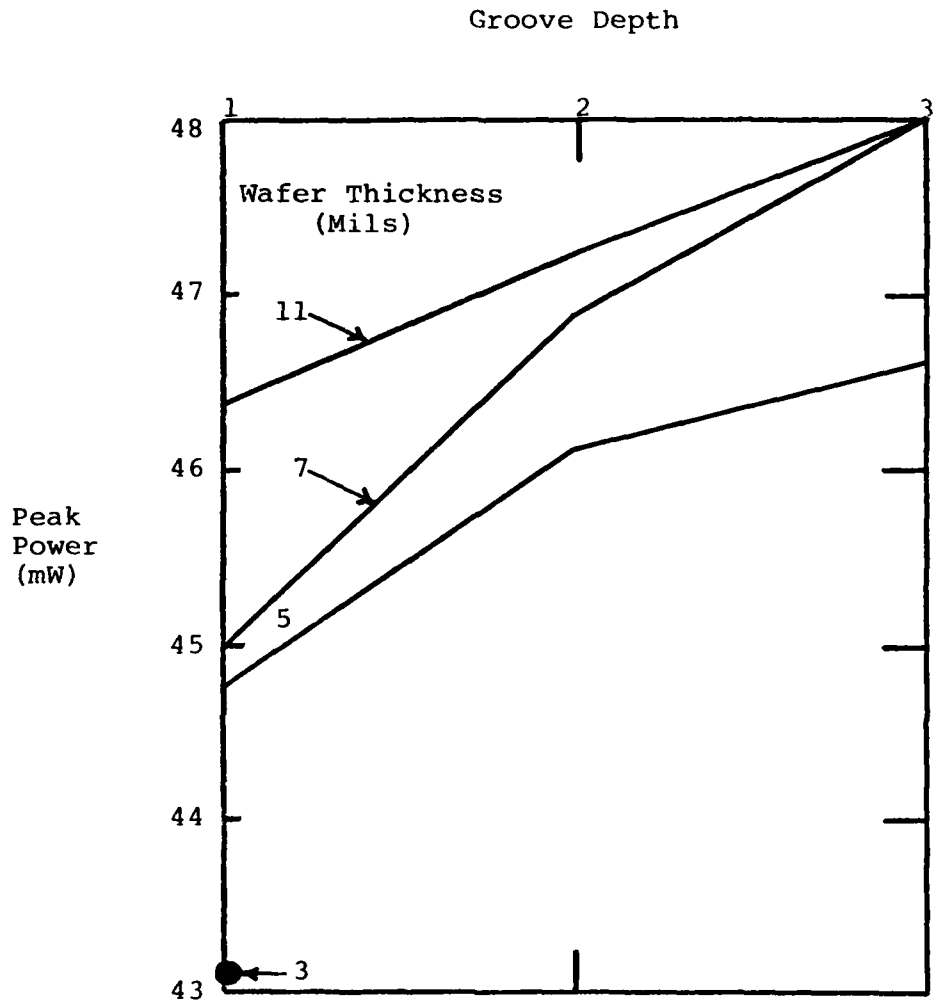
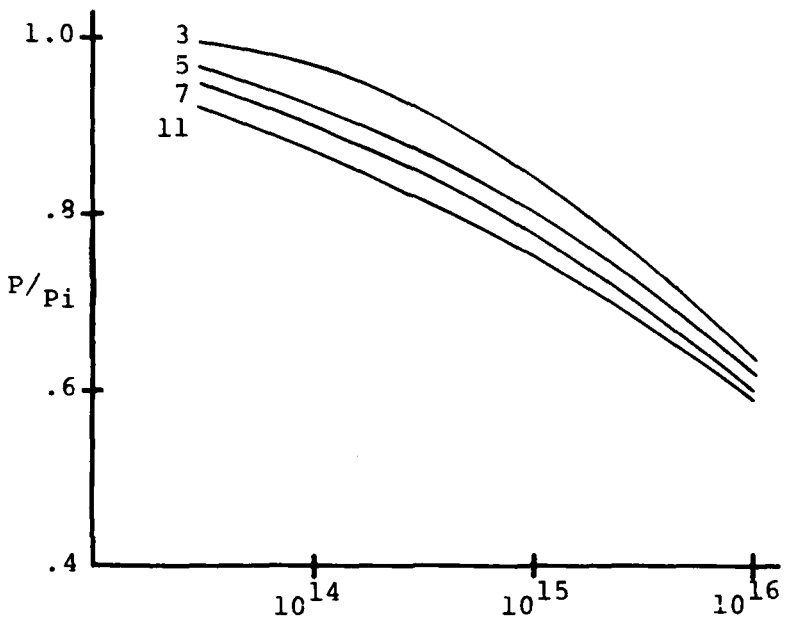
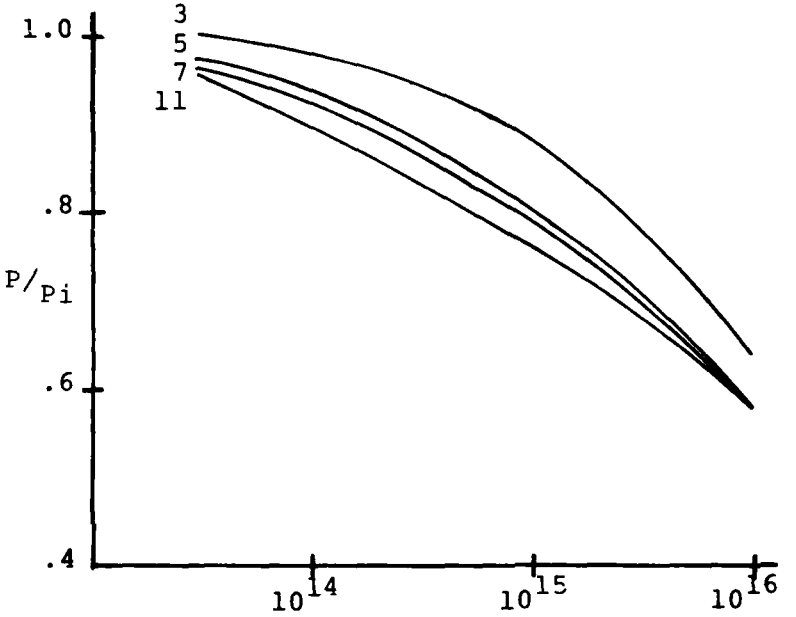


Figure 20. End of Life (10^{16} 1 MeV e^-/cm^2 Peak Power as a Function of Wafer Thickness and Groove Depth (Average of 2 & 10 ohm-cm Bulk Resistivities)

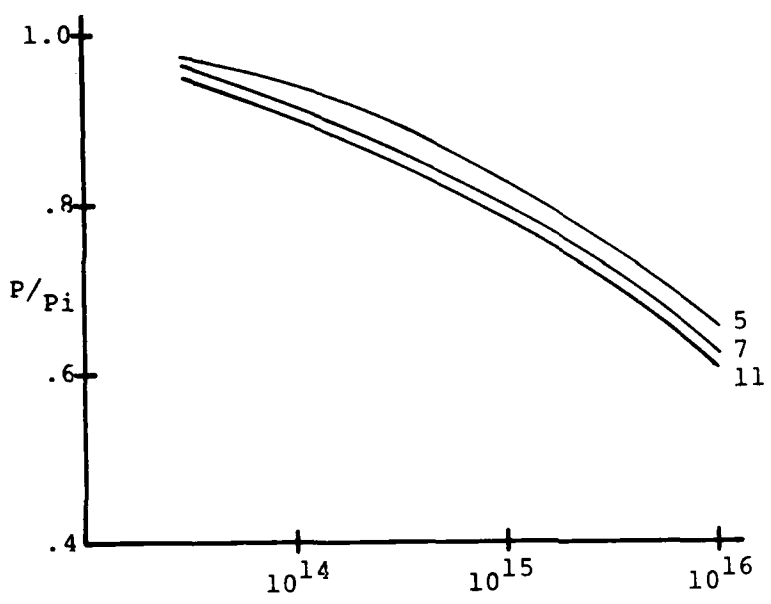


Cummulative Fluence
(1 Mev Electrons)
a. 10Ω-cm.

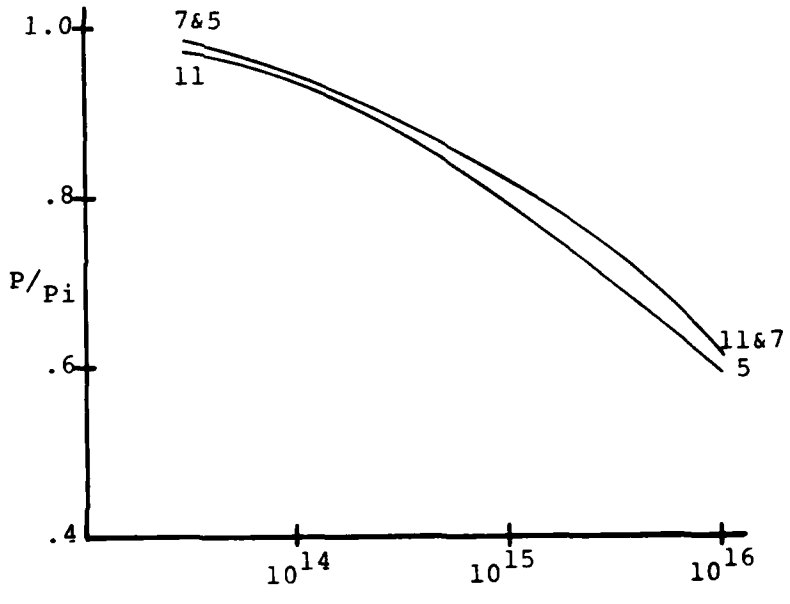


Cummulative Fluence
(1 Mev Electrons)
b. 2Ω-cm.

Figure 21. Relative Maximum Power Point (P/P initial) vs. Fluence for 1 mil Deep VJ Cells as a Function of Substrate Thickness



Cummulative Fluence
(1 Mev Electrons)
a. 10Ω-cm.



Cummulative Fluence
(1 Mev Electrons)
b. 2Ω-cm.

Figure 22. Relative Maximum Power Point (P/P initial) vs. Fluence for 3 mil Deep VJ Cells as a Function of Substrate Thickness

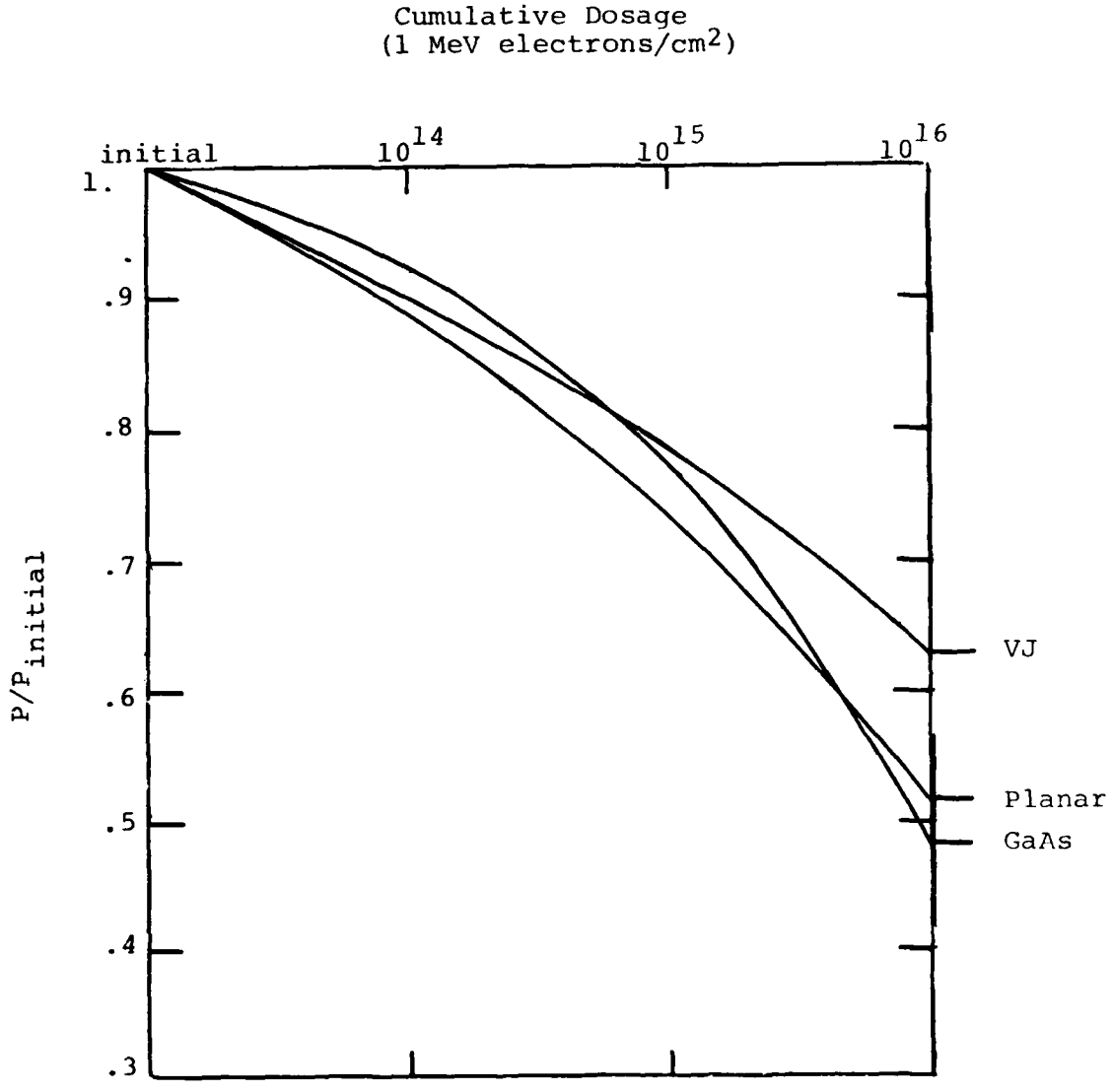


Figure 23. Relative Maximum Power Point ($P/P_{initial}$) vs Fluence for VJ Cell, Silicon Planar Cell, and GaAs Cell.

to a 25% power loss for an equivalent 11 mil thick VJ cell. These thin VJ cells offer significant advantages in EOL power to weight ratio

Figure 23 compares a VJ cell with a silicon planar cell and with an (AlGa)As-GaAs cell (Ref. 6). The VJ cell has 2 mil grooves, 11 mils wafer thickness and 10 ohm-cm resistivity. The planar cell is 2 ohm-cm resistivity.

Figure 23 shows that VJ cells are more radiation tolerant than both planar cells and advanced GaAs cells.

5. THERMAL ANNEALING

Radiation damage can be removed by thermal annealing while the array is in space. We have annealed irradiated cells at 400°C and plotted the electrical ouput as a function of time, shown in Figures 24a, b, and c. All cells had two mil grooves, and were irradiated to 10^{15} 1 MeV electrons/cm^2. Figures 24a and 24b each refer to an average of four cells of 11 mils thickness, of two and ten ohm-cm resistivity, respectively. Figure 24c refers to a single cell, 5 mils thick of 2 ohm-cm resistivity.

The cells had Ti/Pd/Ag contacts. All cells show some improvement. We feel that much greater gains may be possible using high temperature contacts. The annealing that occurred on the cells depicted in Figure 24 is counterbalanced by degradation due to the contacts sintering through the junction. Our work with high temperature contacts is described in Section 3.7.

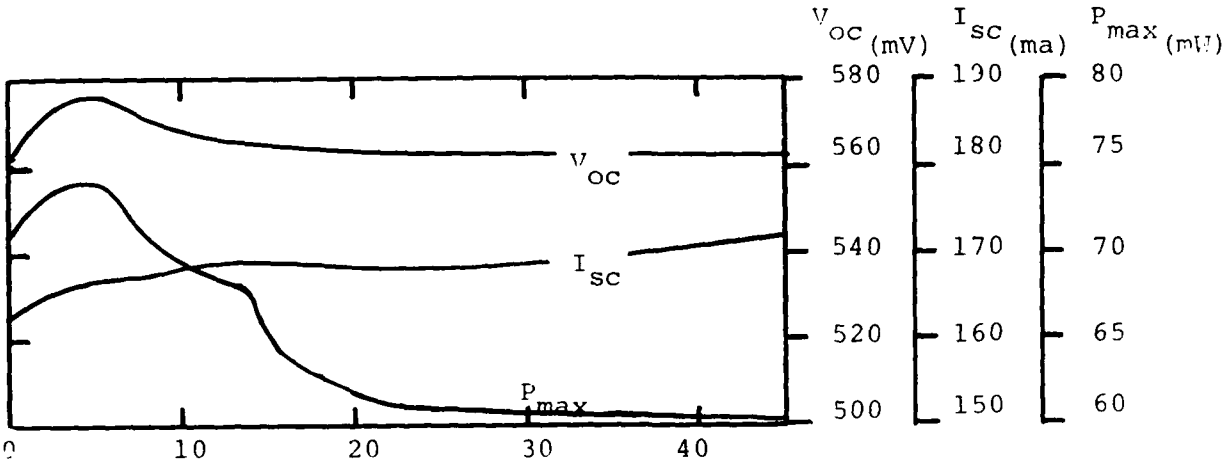


Figure 24 a. 2 ohm-cm. 11 mil wafer

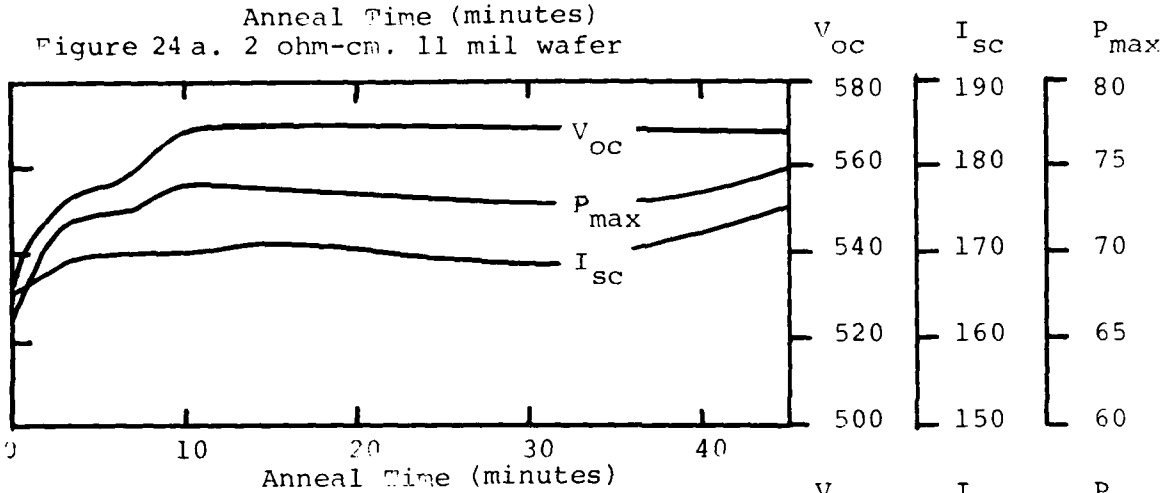


Figure 24 b. 10 ohm-cm, 11 mil wafer

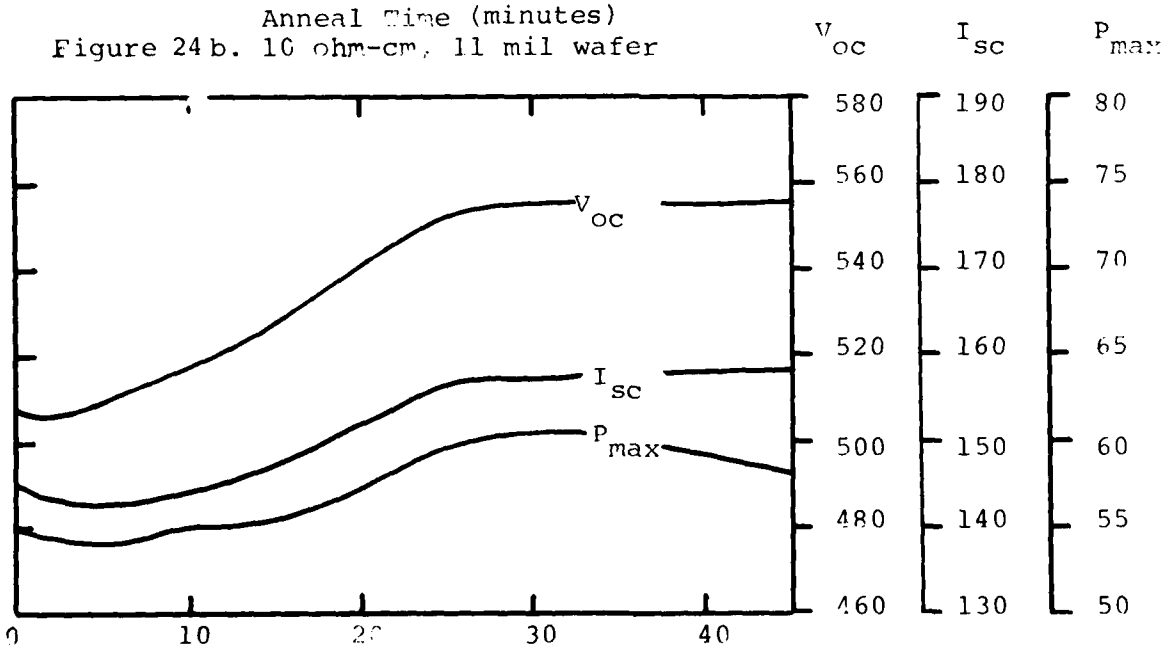


Figure 24 c. 2 ohm-cm, 5 mil wafer

6. OPTICAL CHARACTERISTICS

The vertical junction structure results in a higher absorptance and emittance than seen for planar cells. Table 8 summarizes the results of such measurements on new-geometry cells with 25-, 50-, and 75-micron deep grooves.

TABLE 8

OPTICAL PROPERTIES OF NEW-GEOMETRY CELLS WITH CERIA-DOPED COVERS

Groove Depth (Microns)	ϵH	α	$\alpha/\epsilon H$
25	0.857	0.921	1.07
50	0.854	0.94	1.10
75	0.854	0.929	1.09

The α/ϵ ratios are typical of those obtained from planar (violet type) cells and are appreciably lower than those obtained from pyramid-textured cells (Reference 7). Therefore, under equivalent deployment conditions, the VJ cells will operate at a lower temperature than other high-efficiency textured cells.

An interesting phenomenon is that the VJ cell current increases for small tilt angles. This is particularly evident at the end of life, as shown in Figure 25. The explanation is that when the cell is tilted, light that enters the groove must reflect from the groove walls several times before reaching the bottom, which enhances light absorption in the radiation tolerant walls. The percentage increase in power

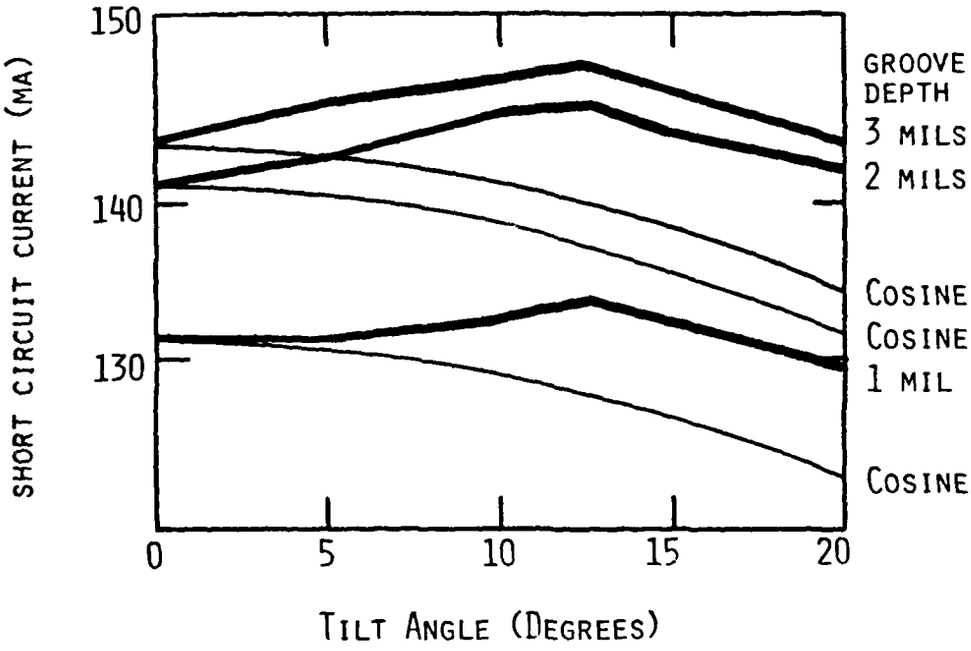


FIGURE 25. SHORT CIRCUIT CURRENT VS. TILT ANGLE. CELL SPECIFICATIONS: 10 OHM-CM, 11 MILS THICKNESS, 10^{16} 1 MEV ELECTRONS/CM^2 IRRADIATION.

between 0^{o} and 12.5^{o} tilt is 2.3%, 4.5% and 9.1% for 1,2 and 3 mil groove depths, respectively. The ratio of initial power under direct normal illumination to EOL power (10^{16} 1 MeV e^{-}/cm^{2}) at 12.5^{o} tilt is 59.6%, 64.9% and 67.2% for 1, 2, and 3 mil deep grooves, respectively. Therefore, the VJ cell has the capability of providing even more end-of-life power by proper orientation.

7. HIGH-TEMPERATURE CONTACTS

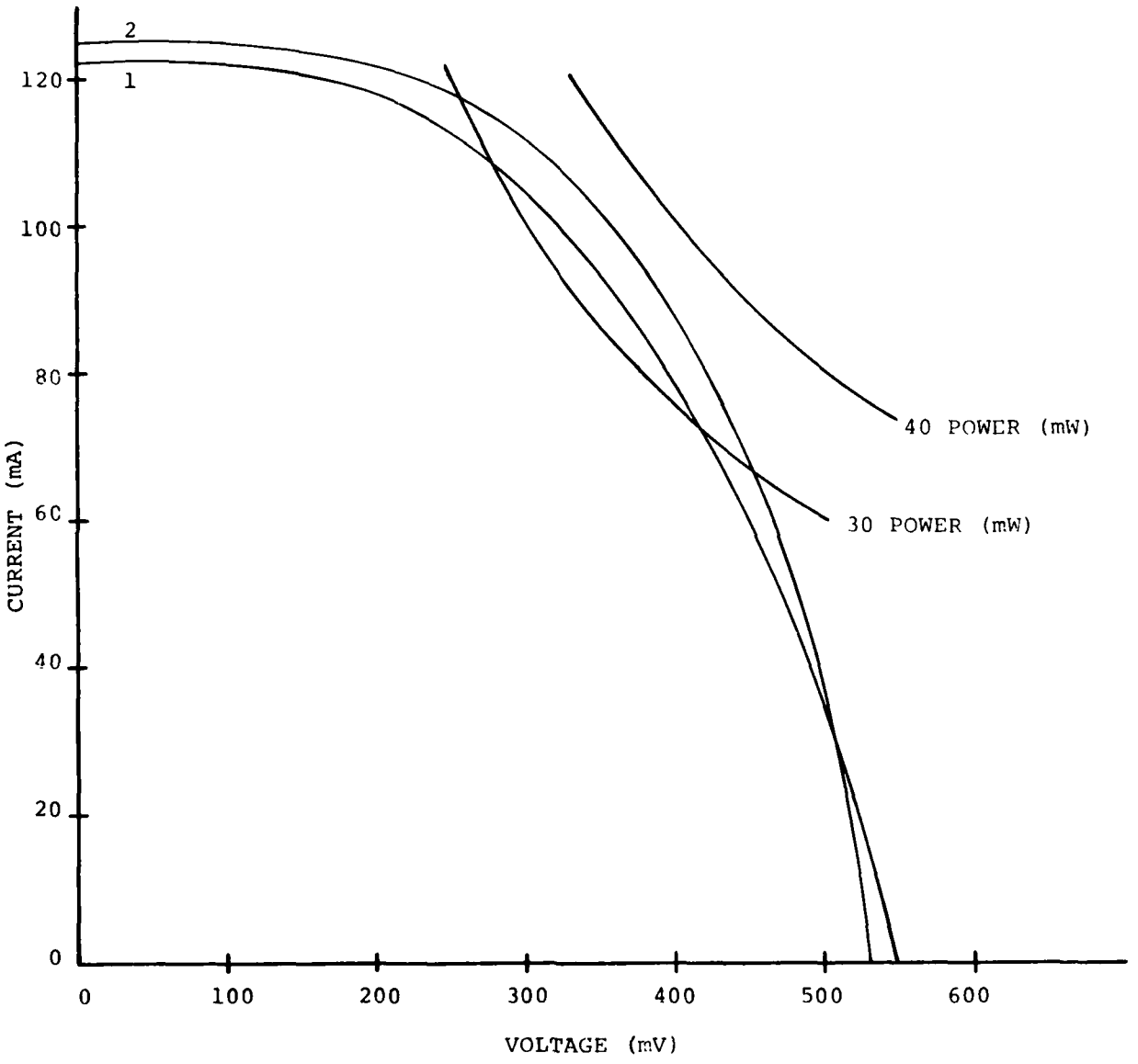
Typically, silicon solar cells for space applications have metallization contacts of Ti-Pd-Ag or Cr-Au-Ag. These contact systems cannot operate at temperatures above $450^{o}C$, even for short periods, without penetration of the junction and subsequent loss of fill factor. This temperature limit is quite restrictive in light of present requirements for cells that can have electrostatic bonded covers applied, can be annealed after radiation damage and can be hardened against laser damage. This section describes our preliminary efforts to develop a cell metallization that can withstand a high-temperature soak at $600^{o}C$ for 5 minutes in vacuum.

The metal placed in contact with the silicon must not penetrate the surface at $600^{o}C$, but must make good electrical and mechanical contact with the silicon. Materials commonly considered for solar cell metallization include Ti, Pd, Cr, Ag, Ni and Cu, but all will penetrate the junction at $600^{o}C$.

We have identified two materials, tantalum and molybdenum, that can be used as the material in contact with the silicon without degrading cell characteristics. These are refractory metals that must be sintered at a high temperature in order to assure good adhesion. This sintering can be done in vacuum or an inert atmosphere. We have used a helium atmosphere for sintering. The sintering has been done for one minute at 600°C after Ta or Mo evaporation and before evaporation of additional metals used for environmental resistance and current conduction.

The additional metal layers consisted of chromium/gold. The bilayer was evaporated, then the cells were gold plated to increase the current-carrying ability of the contacts.

Finished cells were tested, then sintered at 600°C for one minute, then retested. The results are shown in Figures 26 and 27. These results are initial experiments and were done on planar wafers. The pre-sintered cells did not have sharp IV curves; nonetheless, the results show promise. Also, while gold was used on these cells, it is possible that lower cost silver could be used instead.



Planar 1 Presinter
2 Post Sinter

Figure 26. MoCrAu Contacts

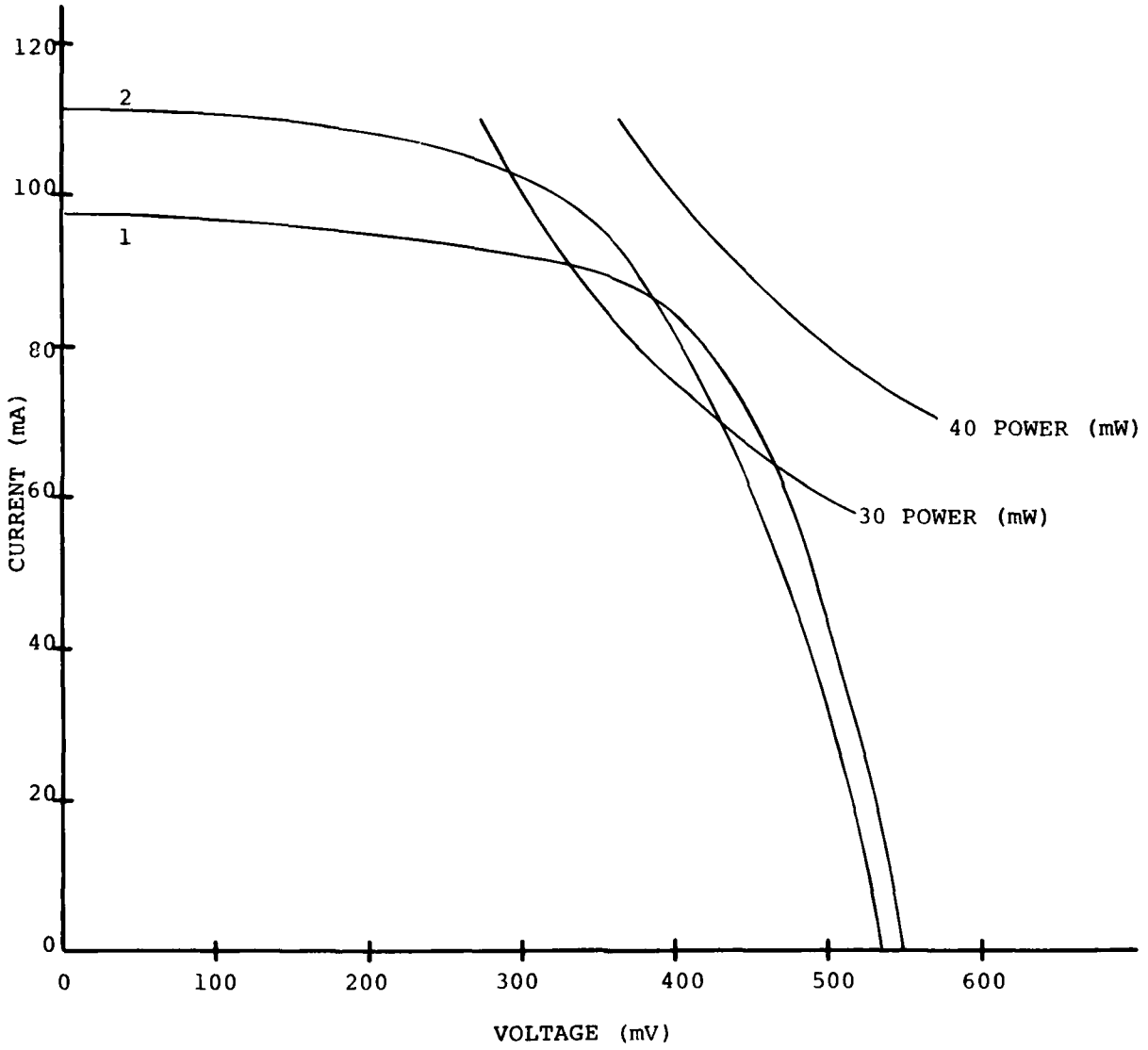


Figure 27. TaCrAu Contacts

SECTION 4
CELL MODELING

Because of its complex structure, the VJ cell requires the development of a two-dimensional carrier diffusion model. The approach taken to develop the model is (1) define the appropriate equations and boundary conditions for carrier concentration at every point in the cell cross-section, (2) develop a numerical technique (relaxation) to perform the numerical analysis, and (3) employ a computer to perform the analysis. Details are given in the following subsection.

There is a set of parameters that are not known with certainty. For the carrier diffusion model, the unknown parameters are back surface recombination velocity and distribution of light in the grooves. There are other unknown parameters that are used to model cell performance but which are not part of the carrier diffusion model, i.e., front surface diode current, light loss due to reflection and contact shadowing, and series and shunt resistance. All the unknown parameters can be deduced by comparing the predictions of the model for a varied set of cells with the actual electrical measurements for the set. The set of programs used to find the best fit between the model and actual measurements is described in the second subsection. The fitting programs have been written but application of the programs could not be completed within this contract.

Nonetheless, an understanding of VJ cells can be gained from the carrier diffusion model alone. The results for a variety of VJ cell structures are given in the third subsection.

1. CARRIER DIFFUSION MODEL

The geometry of the VJ structure to be considered in the model is shown in Figure 28. A number of simplifying assumptions have been made:

a. The n^+ and p^+ regions are so thin that any carrier generation in these regions can be neglected.

b. The electric field is confined to the depletion region and can be ignored in the bulk p region.

In the bulk p region the diffusion equation can then be written:

$$\nabla^2 n + G/D - n/L^2 = 0 \qquad (1)$$

where n = free electron density in p-type silicon, excess above equilibrium value, n_o.
G = carrier generation rate due to illumination
D = diffusion constant
L = diffusion length of minority carrier

The following boundary conditions have been used:

- at the n^+/p front junction:

$$n = n_o(\exp(Vq/kT) - 1) \qquad (2)$$

- at the p-p+ back junction there is a given surface recombination velocity such that:

$$\nabla n = nV_s/D. \qquad (3)$$

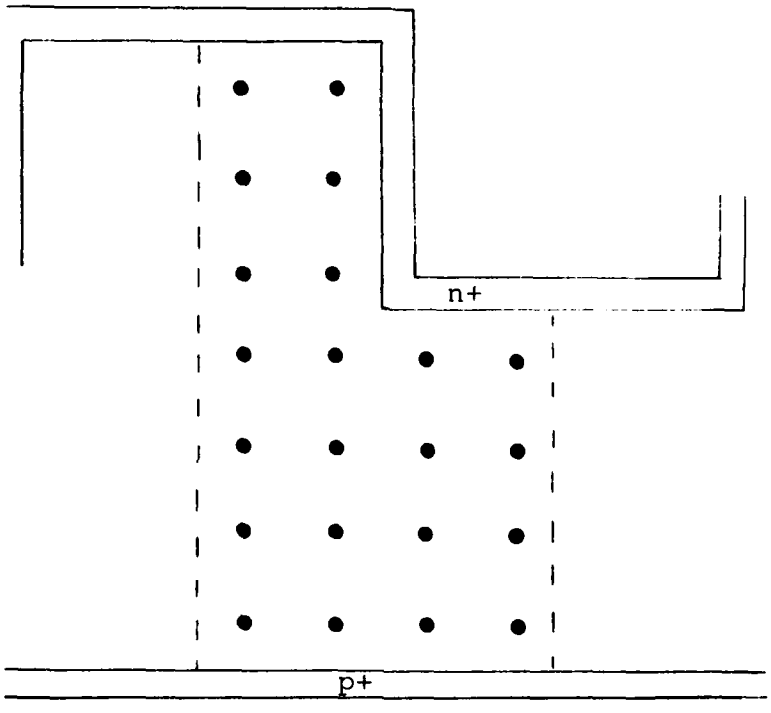


Figure 28. Lattice for Vertical Junction Solar Cell Modeling.

- at the symmetry boundaries designated by surfaces C and D in Figure 26, the net flow of minority carriers is zero:

$$\nabla n = 0. \tag{4}$$

This set of differential equations must be solved to determine values of the minority carrier concentration at all points within the bulk. Then the current density can be determined by solving for the current density given by:

$$\vec{J} = qD\vec{\nabla}n. \tag{5}$$

The value of the current density as a function of position along the n^+/p junction boundary must be found and the cell current determined by integrating over the junction surface. This technique is applicable to VJ cells at Air Mass Zero, but may not be applicable at higher concentrations when the current in the bulk generates an electric field that significantly modifies the diffusive flow.

To solve the set of equations a numerical technique, the relaxation method, has been implemented as a computer program. In the relaxation method the region is divided into discrete points and the equations are written in

terms of nearest-neighbor values. Figure 29 indicates the type of labeling used for a particular point and its adjacent neighbors. At point $n_{i,j}$ the diffusion equation can then be written:

$$(n_{i+1,j} + n_{i-1,j} - 2n_{i,j}) / \Delta x^2$$
$$+ (n_{i,j+1} + n_{i,j-1} - 2n_{i,j}) / \Delta y^2$$
$$+ G_{i,j}/D - n_{i,j}/L^2 = 0 \qquad (6)$$

The determination of the generation rate, G, is based on an algorithm that is repeated eight times. Two parameters -- the absorption coefficient and the incident photon density -- are changed each time the algorithm is repeated. In this manner the air mass zero generation rate is approximated by summing the results of eight discrete wavelength bands. The algorithm traces both a vertical and a horizontal light path. In either case the generation rate is increased at a lattice point based on the amount of light extinguished when passing through the silicon surrounding that point.

One vertical path begins at the wall top and another vertical path begins at the groove bottom. The ray is traced until reaching the back of the cell. The photon density of the vertical ray that enters the groove bottom is reduced from the full incident value by a certain fraction which is assigned, in turn, to the horizontal component. The horizontal component has a photon density equivalent to having the light spread across the entire groove wall. The horizontal light path makes

four transits across the groove walls, then the light path moves vertically through the silicon below the grooves. The four transits across the groove wall represents the fact that light transits a wall several times whether it is internally reflected or exits the wall and enters the adjacent wall.

At a boundary at least one of the adjacent points is outside the lattice. The boundary conditions are used to derive a value for this external point so that the value of the center point can be calculated as usual. Table 9 shows that, for the junction, the carrier density is an exponential function of voltage; for a fixed recombination velocity, the external point carrier density is a linear decrement of the central point value; and for the lines of symmetry, the external and center values are equal.

Equation 6 can be solved for $n_{i,j}$ so that the carrier density at the center point can be derived from the four adjacent points in a way that is consistent with the diffusion equation. The entire lattice is reconciled this way, constituting one computer cycle. The carrier distribution converges to a steady state after several hundred cycles.

TABLE 9

CONTINUOUS AND DISCRETE REPRESENTATIONS OF BOUNDARY CONDITIONS

	Continuous	Discrete
Boundary Condition at Junction	$n = n_o(e^{Vq/kT}-1)$	$n_e = n_J = n_o(e^{Vq/kT}-1)$
Boundary Condition for Surface with Recombination Velocity, V_s	$\nabla n = nV_s/D$	$n_e = n_{i,j}\ (1-(\Delta r V_s/D))$
Zero Current Boundary	$\nabla n = 0$	$n_e = n_{i,j}$
Current at Junction	$\vec{J} = qD\vec{\nabla}n$	$J = (n_{i,j} - n_J)qD/\Delta r$

where n_e = carrier density at an external point

n_J = carrier density at junction

Δr = Δx or Δy depending on the direction of displacement of two points

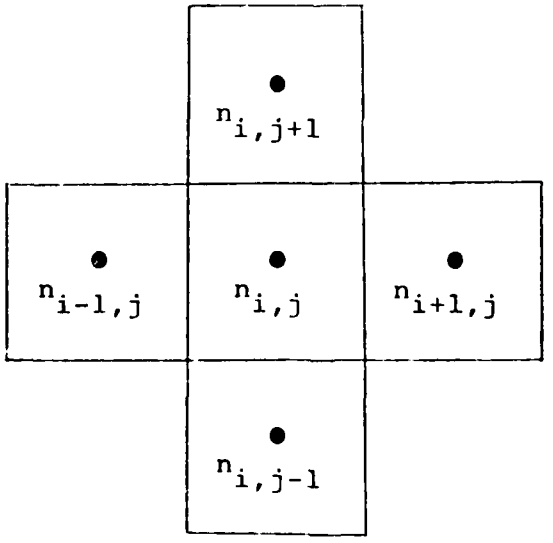


Figure 29. Points Adjacent to $n_{i,j}$

2. FITTING MODEL TO ACTUAL CELL DATA

Some of the parameters used in the modelling of VJ cell electrical output cannot be measured on individual cells. Determining these "hidden" parameters is a prerequisite to making accurate predictions. The hidden parameters can be derived by fitting the model to a set of actual cell measurements.

To find a hidden parameter one must be able to assume that the parameter remains nearly constant over a certain set of cells. For example, consider a set of cells with different thicknesses, known, and similar back surface recombination velocities, unknown. For each cell the predicted short circuit current is compared to the actual measurement for a range of back surface recombination velocities. For each recombination velocity a goodness of fit is derived for the whole set of cells. The recombination velocity that gives the best fit is the most likely value. In actual practice there are several known parameters and many unknown parameters. Furthermore, due to variations in the cells the hidden parameters cannot be determined precisely but rather a likely range is determined.

There are three major computer programs used in the fitting procedure. The first program solves the two dimensional diffusion equation for photogenerated minority carriers. The program, which will be called the Diffusion Model, was described in the previous subsection. The input parameters are shown in Table 10. The output is the light generated current.

TABLE 10

INPUT PARAMETERS TO DIFFUSION MODEL

1) Wall Width
*2) Diffusion Length
*3) Back Surface Recombination Velocity
*4) Distribution of Light in Grooves
5) Groove Depth
6) Wafer Thickness
7) Wavelength Band of Illumination
8) Applied Voltage
9) Groove Pattern Step and Repeat
10) Dopant Density

*Hidden Parameters

A driver program was written to cycle the Diffusion Model through a set of cases. For the purpose of fitting the model to measured data the step and repeat parameter (Item 9 of Table 10) was held fixed since cells were made from a single mask pattern.

The Diffusion Model was shown to obey the diode equation, Equation 7.

$$I = I_{sc} - I_o(e^{Vq/kT}-1) \qquad (7)$$

I_o for the silicon bulk is inversely proportional to the dopant density hence can be transformed without the Diffusion Model. Consequently, the dopant density (Item 10) was held fixed.

The wavelength band (Item 7) involved two cases, AM0 and low pass red. For AM0 several applied voltages (Item 8) were used as input from which I_o was later derived. For red illumination only zero applied voltage was used. In sum, the input variables were Items 1-8 and the output was current.

The output from the diffusion model was then processed to derive a file with six input parameters, Items 1-6; and

three outputs: short circuit current at AM0, short circuit current under red light, and I_o for the silicon bulk.

The Diffusion Model requires extensive computation so that it cannot be used directly to explore the fit to actual measurements using a successive approximation search. Instead, the data from the Diffusion Model was used to generate three polynomial interpolation functions: one for I_{sc} AM0, one for I_{sc} red, and one for I_o. For example, the back surface recombination velocity input to the Diffusion Model might have been 20. and 200. cm/sec. The case of 100. cm/sec can then be estimated from the interpolation function much more rapidly than from the Diffusion Model. The second major program in the fitting sequence is one that derives the interpolation function.

The form of the interpolation polynomial can be varied to suit a particular experiment. For the present work the terms have the forms shown in Table 11. The variables u, v, w, x, y, z refer to the first six items of Table 10.

TABLE 11

POLYNOMIAL TERMS

$$
\begin{aligned}
&a_1u + a_2v + a_3w + a_4x + a_5y + a_6z \\
&+ a_7u^2 + a_8uv + a_9uw + a_{10}ux + a_{11}uy + a_{12}uz \\
&+ a_{13}v^2 + a_{14}vw + a_{15}vx + a_{16}vy + a_{17}vz \\
&+ a_{18}w^2 + a_{19}wx + a_{20}wy + a_{21}wz \\
&+ a_{22}x^2 + a_{23}xy + a_{24}xz + a_{25}y^2 + a_{26}yz + a_{27}z^2 \\
&+ a_{28}uvw + a_{29}uvx + a_{30}uvy + a_{31}uvz + a_{32}uwx + a_{33}uwy \\
&+ a_{34}uwz + a_{35}uxy + a_{36}uxz + a_{37}uyz \\
&+ a_{38}vwx + a_{39}vwy + a_{40}vwz + a_{41}vxy + a_{42}vxz + a_{43}vyz \\
&+ a_{44}wxy + a_{45}wxz + a_{46}wyz + a_{47}xyz + a_{48} \\
&= \text{an electrical measure } (I_{sc} \text{ AM0, } I_{sc} \text{ red, or } I_o \text{ bulk})
\end{aligned}
$$

Multiple linear regression can be used to find the interpolation polynomials. The polynomials are not linear in six variables but linear in 47 variables (the 48 terms of Table 11 less the constant term). The program that derives the interpolation polynomials first takes each case of the Diffusion Model and converts the point in six parameter space into a point in 47 parameter space. The expanded vector and the corresponding outputs for all cases are fed to a multiple linear regression routine to derive a_{1-48}.

The third major computer program, which I will call the Fitting Program, incorporates both a complete cell model and a procedure for finding the best fit to measured cells. Some additional hidden paramteres are introduced: front diode current, reflection loss, red filter reflection, series resistance, and shunt resistance. The complete set of hidden parameters are listed in Table 12.

TABLE 12

HIDDEN PARAMETERS

1) Back Surface Recombination Velocity
2) Distribution of Light in Grooves
3) Front Surface Diode Current
4) Diffusion Length
5) Reflection Loss
6) Adjustment of Red I_{SC} for Filter Used in Measurement
7) Series Resistance
8) Shunt Resistance

Not all of the parameters in Table 12 are actually hidden, but all parameters of Table 12 were not measured on every cell. Consequently, for a set of cells an average value must be assumed to apply to all cells of the set as is done with hidden parameters. In practice, two sets have been compiled: two ohm-cm and ten ohm-cm.

The Fitting Program procedure involves a set of nested loops by which the hidden parameters are varied. For each particular hidden parameter vector there is an associated goodness of fit value which is the sum over all cells of the absolute value of the difference between electrical measurement and model prediction.

Besides the hidden parameters given in Table 12, three more parameters are needed to predict electrical performance. These are cell dependent parameters: groove depth, wafer thickness, and bulk resistivity. The first step is to solve the three interpolation polynomials based on the first six items of Table 10. These six parameters refer directly to either hidden parameters or cell dependent parameters, except for the wall width. The wall width is calculated from the groove depth based on the observed relationship. The three interpolation functions give values for I_{sc} AM0, I_{sc} red,

and I_o bulk. In order to compare the predictions with actual cell measurements the predictions must take the form of I_{sc} AMO, I_{sc} red, P_{max}, and V_{oc}.

The first step is to calculate $I_{o,total}$ of the diode equation. The $I_{o,total}$ is the sum of I_o bulk, which is corrected for the cell's bulk resistivity, and I_o from the front surface. The I_o from the front surface is the product of the front diode current per square cm (a hidden parameter) times the surface area (which can be derived for each cell).

I_{sc} red is then calculated from these parameters: I_{sc} red from the interpolation polynomial, $I_{o,\ total}$, overall cell reflection, correction for red filter used in measurement, series resistance and shunt resistance.

I_{sc} AM0, P_{max}, and V_{oc} are derived by tracing out an IV curve (numerically in the computer). The parameters used for the calculation are: I_{sc} AM0 from the interpolation polynomial, $I_{o,total}$, overall cell reflection, series resistance, and shunt resistance.

When all cells and all hidden parameters have been considered by the computer then for each hidden parameter vector

there are four goodness of fit measures; one for each: I_{sc} AM0, I_{sc} red, P_{max}, and V_{oc}. Dividing by the number of cells the goodness of fit has the same units as the electrical parameters, for example millivolts for V_{oc}. Now suppose two hidden parameter vectors have a fit of 1 mV and 2 mV. The accuracy of the actual measurements is only about 3 mV so that both parameter vectors are valid estimates. The program's results are arranged so that for each hidden parameter a histogram is formed in which for each value the number of cases (parameter vectors) with a fit below the measurement error are given. These histograms are used to determine a range of possible values for each hidden parameter.

It is not practical to compute more than about 250 cases at one time due to limits on computer resources. Four values for each of four parameters reaches this limit. To obtain better resolution the program is run more than once with successively smaller variable increments, and with different choices for which parameters to vary or hold fixed.

The Fitting Program has been used on a test basis and has been shown to operate correctly. We have been unable to completely implement the extensive computations required to resolve the hidden parameters during this contract, due to schedular and financial restraints.

3. I-V MODELING

The carrier diffusion model has been employed to generate idealized (no series or shunt resistance included) I-V curves for a variety of VJ structures using various materials characteristics. Figure 28 shows the effect of diffusion length on the I-V curves for one particular cell structure, namely the old geometry with 7.5-micron-wide grooves and 7.5-micron-wide walls. The curves are plotted for 25-micron and 75-micron-deep grooves. Figure 29 shows the effect of diffusion length on the I-V curves for the new geometry with 12.5-micron-wide walls and 5.0-micron-wide grooves. The curves are plotted for 25-micron and 75-micron-deep grooves. Table 13 compares the two geometries. The new geometry results in slightly higher efficiencies as long as the diffusion length is longer than the wall thickness.

These curves (Figures 30 and 31) show that:

- short-circuit current increases with increasing groove depth
- open-circuit voltage decreases with increasing groove depth.

TABLE 13

COMPARISON OF COMPUTER MODEL PERFORMANCE

FOR OLD AND NEW GEOMETRY CELLS

75 Micron Deep Grooves
2 Ω-cm Silicon
300 Micron Thick Substrates

For 2 cm x 2 cm Cell

Diffusion Length		Old Geometry 7.5μ-7.5μ	New Geometry 12.5μ-5.0μ	
250	P_{max}	98	98	mW
	I_{sc}	191	194	mA
	V_{oc}	609	616	mV
100	P_{max}	88	89	mW
	I_{sc}	183	186	mA
	V_{oc}	585	580	mV
40	P_{max}	77	78	mW
	I_{sc}	172	178	mA
	V_{oc}	550	546	mV
16	P_{max}	64	66	mW
	I_{sc}	158	164	mA
	V_{oc}	510	505	mV
6.4	P_{max}	47	47	mW
	I_{sc}	130	128	mA
	V_{oc}	460	460	mV
2.56	P_{max}	25	21	mW
	I_{sc}	77	65	mA
	V_{oc}	420	422	mV

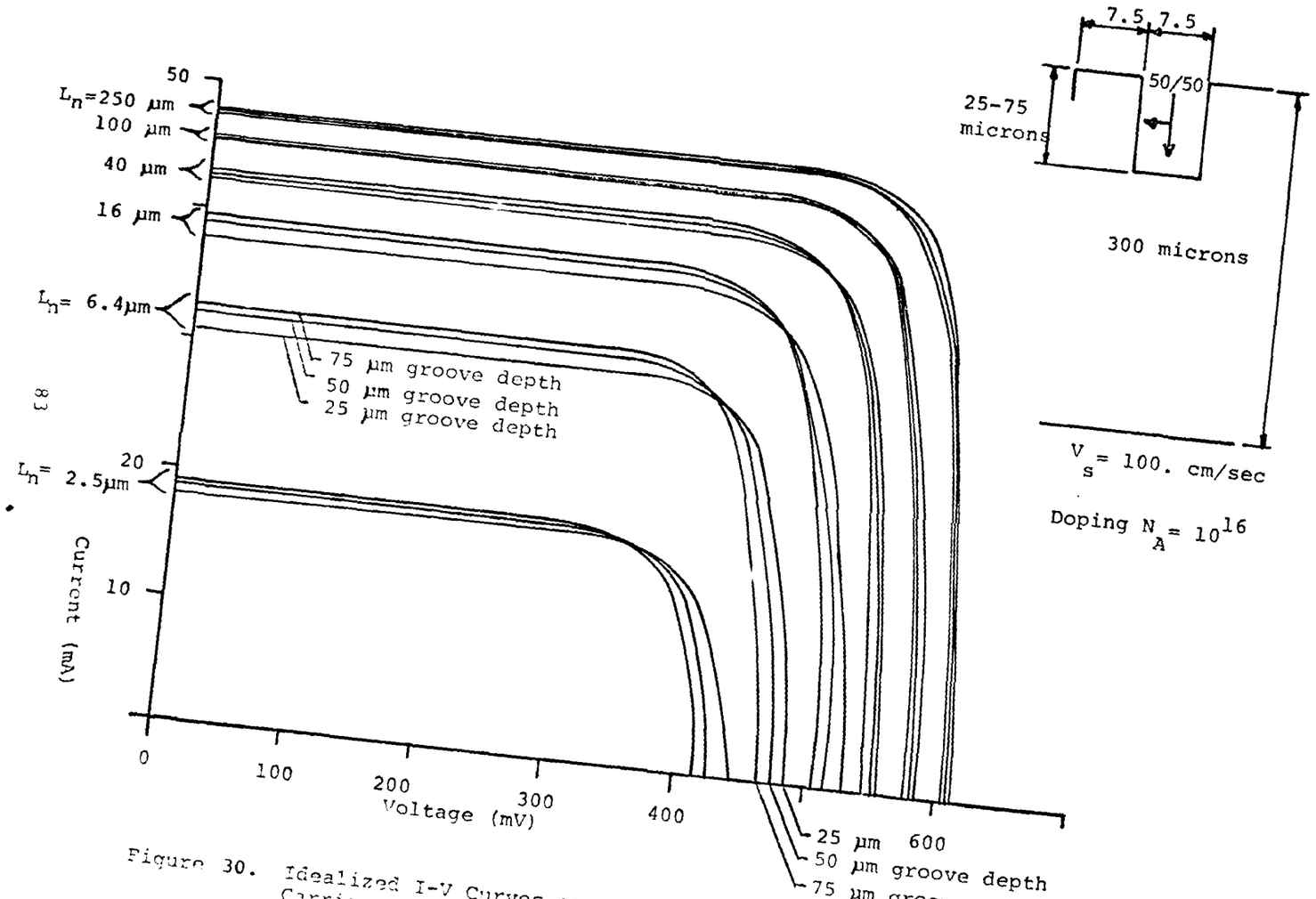


Figure 30. Idealized I-V Curves as a Function of Minority Carrier Diffusion Length - Old Geometry

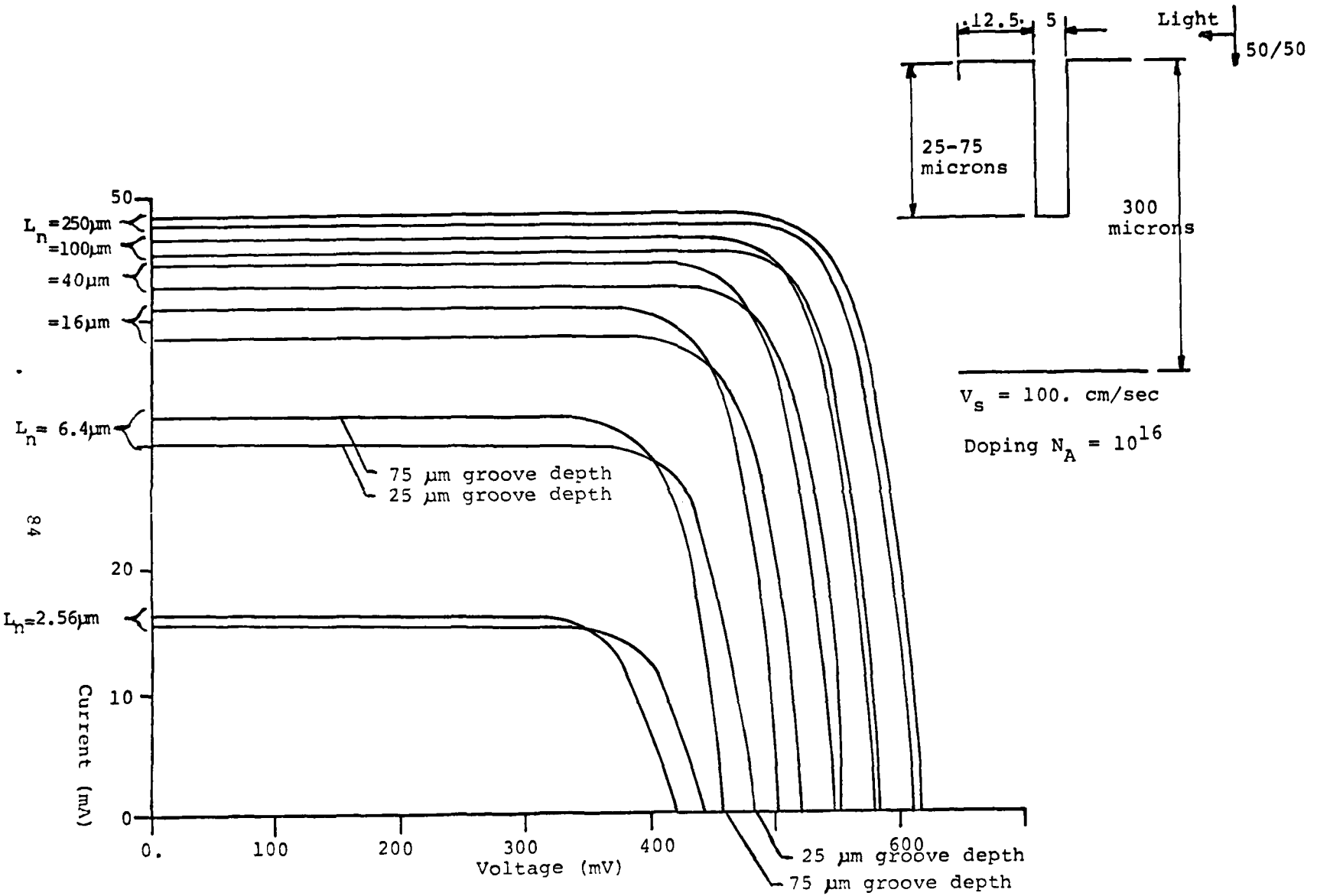


Figure 31. Idealized IV Curves as a Function of Minority Carrier Diffusion Length - New Geometry

These observations agree with the experimental results given in Section 3. However, according to these computer-generated curves, the maximum power is insensitive to the groove depth for a given diffusion length. This has been verified for cells with long diffusion lengths (before irradiation) but, as is shown in Section 3., the cells with deeper grooves are appreciably more radiation-resistant than those with shallow grooves. This discrepancy may be because the simple model assumed that the fraction of light entering the groove walls was independent of groove depth. In reality, the deeper the grooves, the more light enters the walls.

Another parameter that has been investigated using the computer model is the effect of the substrate thickness on cell performance. Figure 32 shows the effect of substrate thickness on the I-V curves of new-geometry cells with 25-micron-deep grooves. For long diffusion lengths, the thicker cells have higher current and lower voltage. The explanation for the trends are that thicker cells convert light into carriers more completely, hence higher current. On the other hand, the voltage is less on a thicker cell because the benefit of the back surface field is lessened. The model predicts that for short diffusion length (post irradiation), the differences between cells of varying substrate thickness disappear. The experimental results, however, indicate that while current does perform as predicted, voltage does not: the cell voltages are independent of substrate thickness.

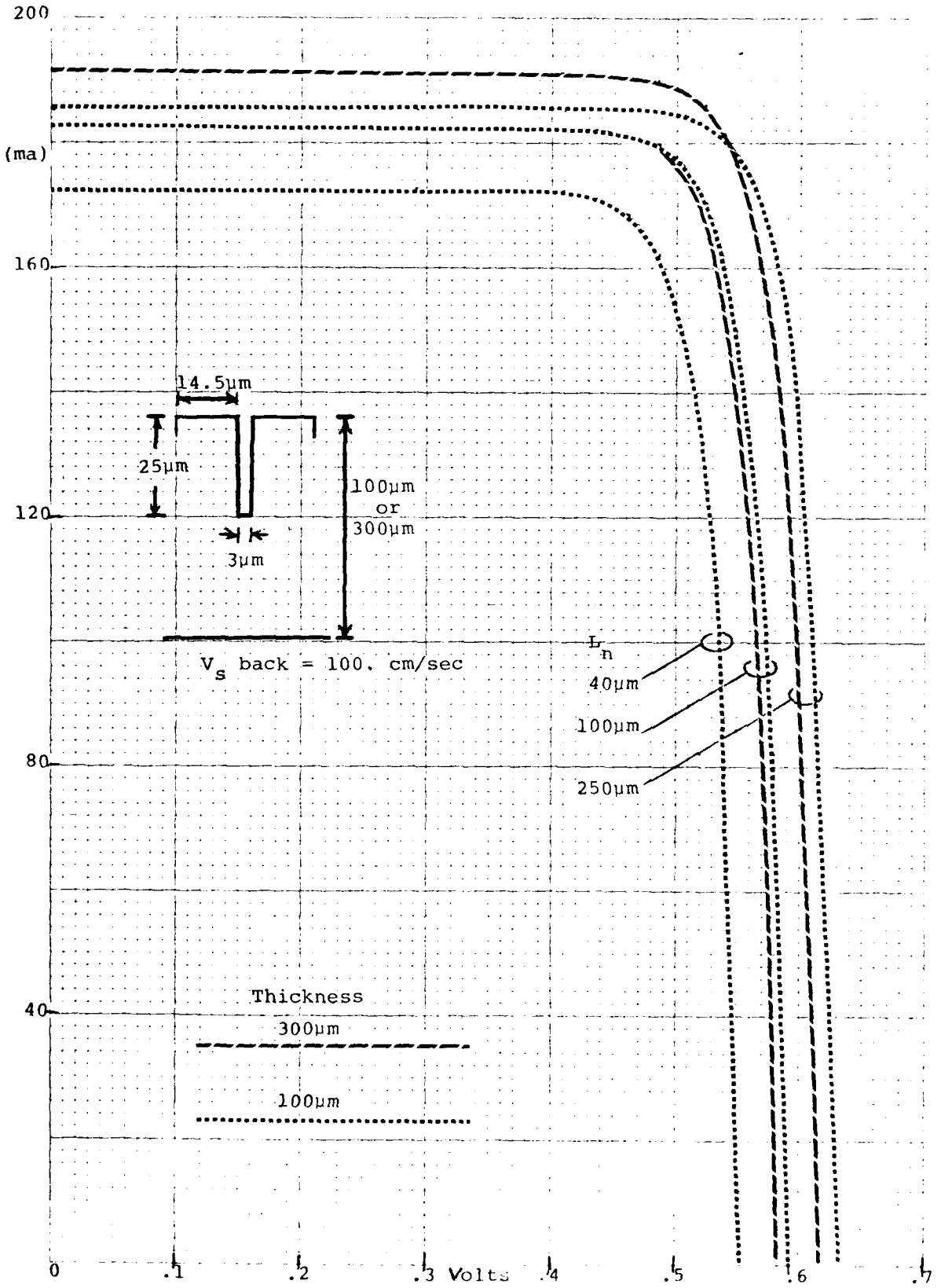


Figure 32. Idealized IV Curves as a Function of Substrate Thickness for a Variety of Groove Depths

The discrepancy between the model and the experimental results appears to be due to the effect of the BSF. In all probability, BSF cannot be modeled using a constant back surface recombination velocity. The BSF is an active junction and its performance can be affected by particulate irradiation.

A simple model of the relationship between junction area and open circuit voltage would suggest a voltage drop of 60mV per factor of ten increase in junction area, as would be predicted for a planar diode for which the photocurrent areal density decreased by a factor of ten. However, the diffusion model shows a much smaller decline of V_{oc} as the junction area is increased due to increased groove depth. The V_{oc} measured on VJ cells shows the same relationship as predicted by the diffusion model. The results are graphed in Figure 33. Line A shows a V_{oc}/junction area of 60 mV/factor of 10. Line B shows the prediction of the diffusion model. Line C shows actual measurements of cells with a 17.5 micron S&R/2.5 groove-window geometry. The diffusion model is offset from actual measurements largely because the diffusion model doesn't include light reflection or contact shadowing, the important point is that the slope of lines B and C are similar.

The explanation for the observed V_{oc}/junction area relationship is depicted in Figure 34. The minority carriers injected from the wall junctions are indistinguishable from light generated minority carriers. The major site of recombination is in the bulk below the grooves and the J_o flowing into there has nearly the same current density as a planar cell.

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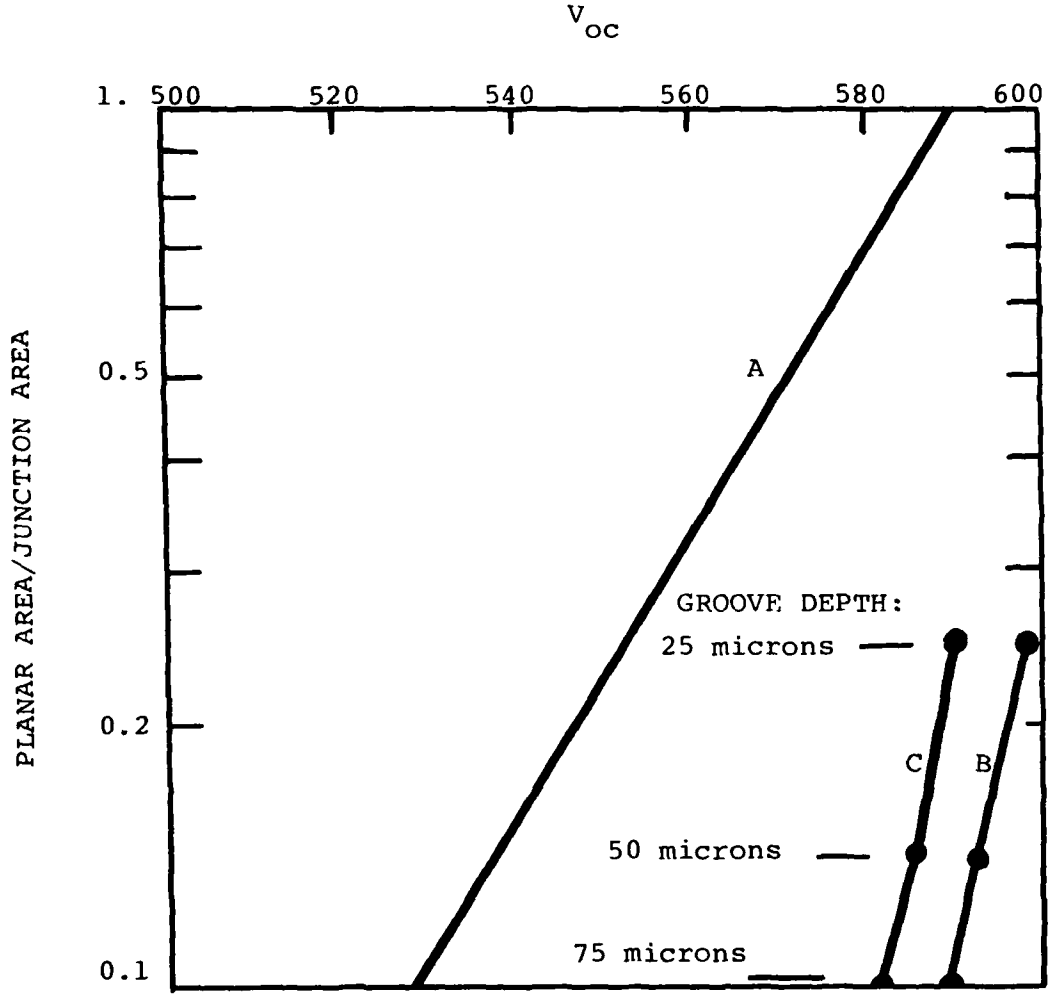

Figure 33. Open Circuit Voltage vs Junction Area

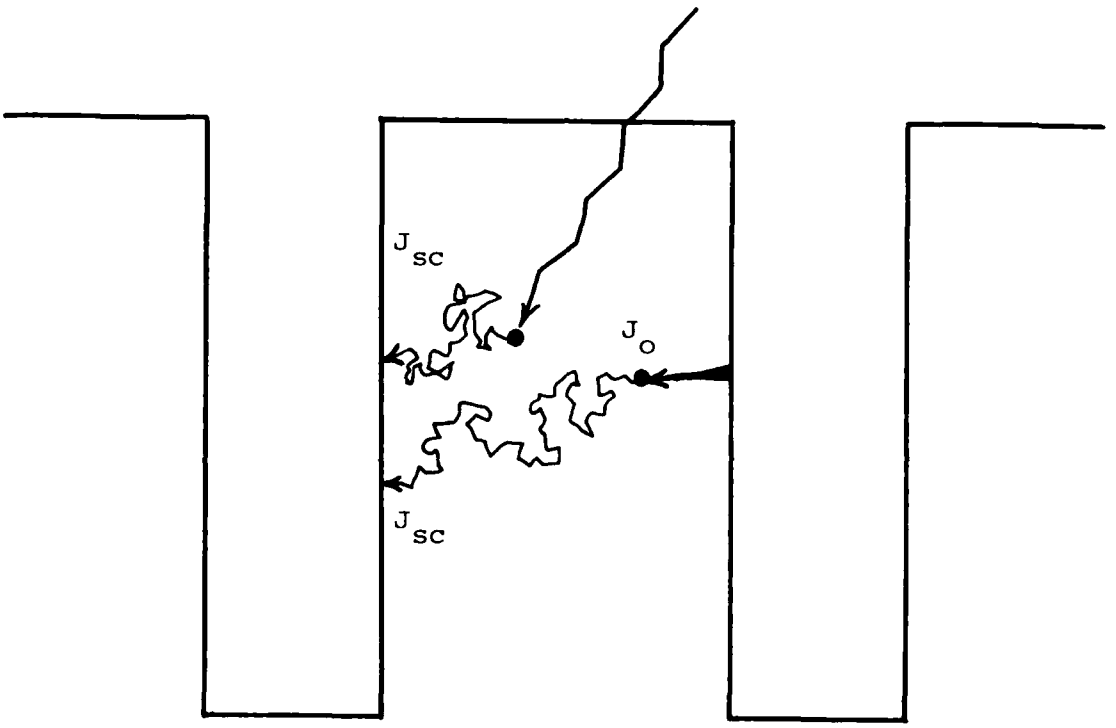

Figure 34. Sources of Short Circuit Current

SECTION 5

CONCLUSIONS

The research done under this contract has resulted in VJ cells with beginning of life efficiency as high as 15.5%. Furthermore, the end of life efficiency is the best that is available from a silicon solar cell. A broad range of process techniques have been developed in order to reach this level.

The technique of using a mechanical stop on the groove mask in conjunction with a flat on the wafer has resulted in a simple method of obtaining precise groove alignment. Another process development of a mechanical nature has been the use of a photoresist mask in order to obtain high quality front contact metallization.

The process times and temperatures have been fine-tuned. For example, the measured open circuit voltage vs groove depth is close to the idealized computer model. This indicates that the recombination velocity at the front surface is relatively low. In regard to the back, aluminum paste alloy and aluminum back surface reflector are two items that have been introduced during this contract.

Double layer AR coating is another improvement introduced during this contract.

What additional improvements can be made to raise the beginning of life efficiency while retaining good radiation tolerance? Primarily, narrower grooves should improve efficiency by allowing shallower grooves hence higher voltage. With a very narrow groove, say one micron, the amount of light entering the lower part of the walls and the silicon below the grooves, can be minimized. By assuring that nearly all the incident light enters the top of the grooves, the same current that we now measure for a particular groove depth should be achievable at a shallower groove depth.

Narrow, shallow grooves have other advantages. For shallow grooves, say 25 microns, VJ cells can be made thin yet sturdy. Consequently, VJ cells should be considered for use in light-weight arrays. Also, with thin shallow grooves it should be possible to use conventional silicone adhesive coversliding techniques.

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